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MS-7640^{ATX} Version: 11



CPU:

AMD AM3 (HT 3.0 up to 5.2GT/s)

System Chipset:

North Bridge : ATI RD890
South Bridge : ATI SB850

On Board Chip:

Super I/O : FINTEK F71889ED
LAN : REALTEK RTL8111DL *2
Audio Codec : REALTEK ALC889
IEEE1394 : VIA VT6315N
USB 3.0 : NEC uPD720200 USB
Extend ESATA : JMICRON JMB363
PCIE Switch : PERICOM PI3PCIE2415ZHE
South Bridge : ATI SB850

Main Memory:

Dual Channel DDRIII x 4 (Max 8GB) (800 / 1066 / 1333/ 1600MHz)

Expansion Slots:

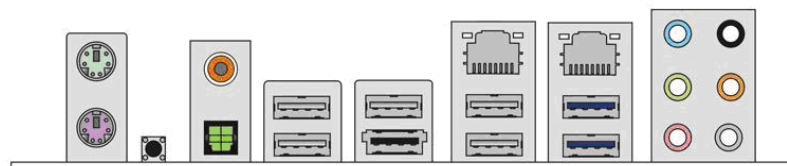
PCI-EPRESS X 16 SLOT x 4
PCI-EPRESS X 4 SLOT x 1
PCI-EPRESS X 1 SLOT x 1
PCI 2.2 SLOT x 1

PWM:

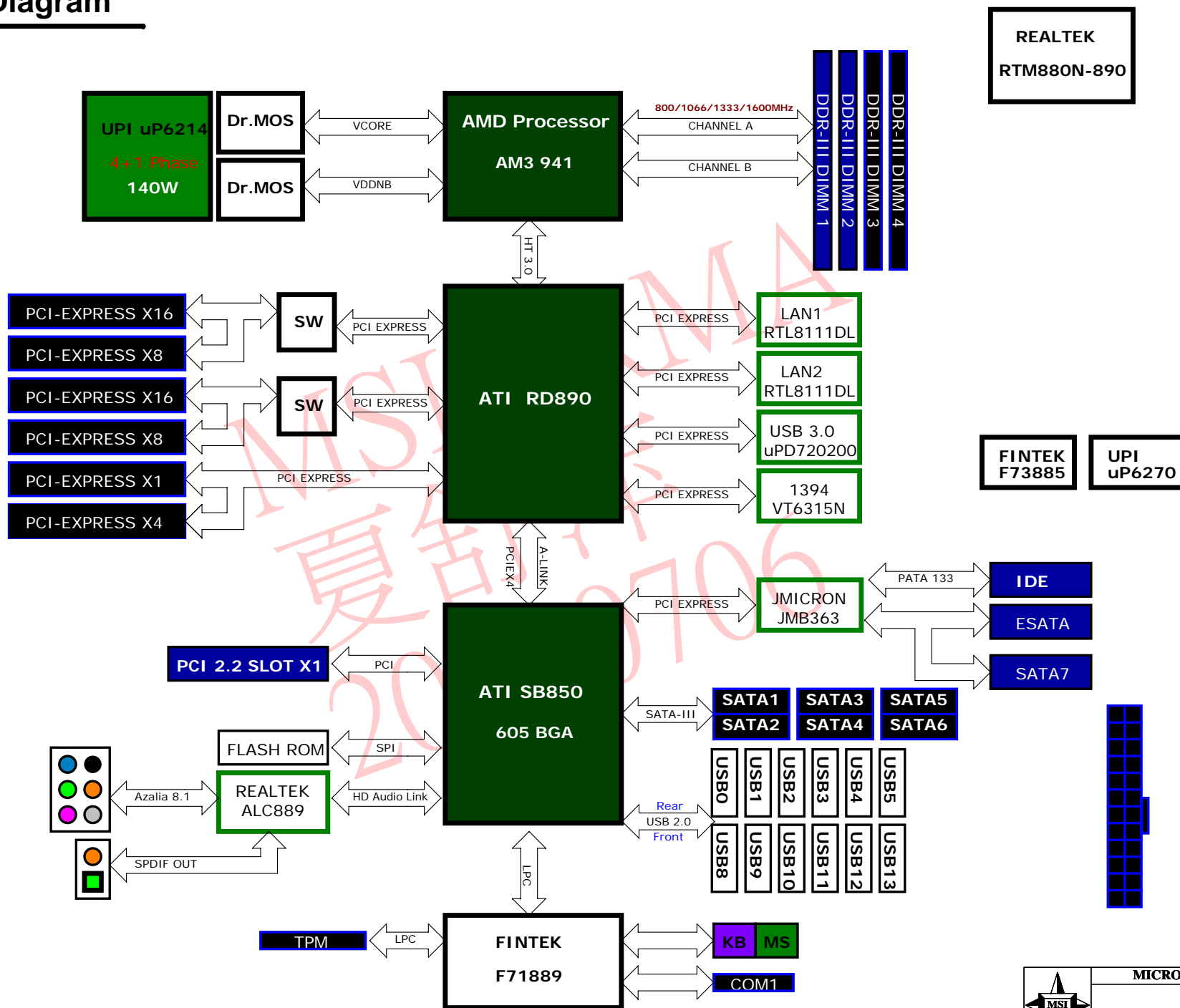
Controller : UPI up6214 + Dr.MOS (4 +1 Phase / 140W)

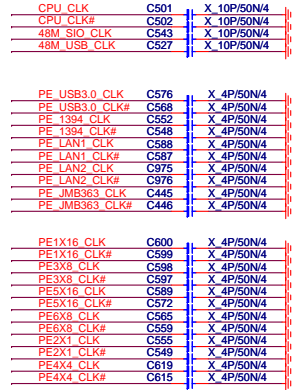
Clock Generator:

Controller : REALTEK RTM880N-890 + ICS9DBL



Block Diagram





7 MEM_MA_DQS_N[8..0] <<<<
7 MEM_MA_DQS_P[8..0] <<<<
7 MEM_MA_DATA[63..0] <<<<
7 MEM_MA_DM[7..0] <<<<
7 MEM_MA_ADD[15..0] <<<<
7 MEM_MA_CHECK[7..0] <<<<

AM3

DIMM 4 MB_CLK 5/3 MB1_CLK 1/0
DIMM 3 MB_CLK 2/4 MB0_CLK 1/0
DIMM 2 MA_CLK 5/3 MA1_CLK 1/0
DIMM 1 MA_CLK 2/4 MA0_CLK 1/0

DATA B

DATA A

8 MEM_MB_DM[7..0] <<<<
8 MEM_MB_ADD[15..0] <<<<
8 MEM_MB_CHECK[7..0] <<<<
8 MEM_MB_DATA[63..0] <<<<
8 MEM_MB_DQS_N[8..0] <<<<
8 MEM_MB_DQS_P[8..0] <<<<

CPU1B

TP61 AG21 MA_CLK_H7
TP57 AG20 MA_CLK_L7
TP53 AE20 MA_CLK_H6
TP56 AE19 MA_CLK_L6
U26 MA_CLK_H5
U27 MA_CLK_H4
W27 MA_CLK_L4
W26 MA_CLK_L3
W25 MA_CLK_H3
U24 MA_CLK_H2
U24 MA_CLK_L2
G19 MA_CLK_H1
H19 MA_CLK_L1
G20 MA_CLK_H0
G21 MA_CLK_L0

AC25 MA0_CS_L1
AA24 MA0_CS_L0
AE28 MA0_ODT1
AC28 MA0_ODT0
AD27 MA1_CS_L1
AA25 MA1_CS_L0
AE27 MA1_ODT1
AC27 MA1_ODT0
TP37 E20 MA_RESET_L

AB25 MA_CAS_L
AB27 MA_WE_L
AA26 MA_RAS_L
N25 MA_BANK2
Y27 MA_BANK1
AA27 MA_BANK0

L27 MA_CKE1
M25 MA_CKE0

MEM_MA_ADD15 M27 MA_ADD15
MEM_MA_ADD14 N24 MA_ADD14
MEM_MA_ADD13 AC26 MA_ADD13
MEM_MA_ADD12 N26 MA_ADD12
MEM_MA_ADD11 P25 MA_ADD11
MEM_MA_ADD10 Y25 MA_ADD10
MEM_MA_ADD9 N27 MA_ADD9
MEM_MA_ADD8 P24 MA_ADD8
MEM_MA_ADD7 P27 MA_ADD7
MEM_MA_ADD6 R25 MA_ADD6
MEM_MA_ADD5 R26 MA_ADD5
MEM_MA_ADD4 R27 MA_ADD4
MEM_MA_ADD3 T25 MA_ADD3
MEM_MA_ADD2 U25 MA_ADD2
MEM_MA_ADD1 T27 MA_ADD1
MEM_MA_ADD0 W24 MA_ADD0

MEM_MA_DQS_P7 AD15 MA_DQS_H7
MEM_MA_DQS_N7 AE15 MA_DQS_L7
MEM_MA_DQS_P6 AG18 MA_DQS_H6
MEM_MA_DQS_N6 AG19 MA_DQS_L6
MEM_MA_DQS_P5 AG24 MA_DQS_H5
MEM_MA_DQS_N5 AG25 MA_DQS_L5
MEM_MA_DQS_P4 AG27 MA_DQS_H4
MEM_MA_DQS_N4 AG28 MA_DQS_L4
MEM_MA_DQS_P3 AG28 MA_DQS_H3
MEM_MA_DQS_N3 C29 MA_DQS_L3
MEM_MA_DQS_P2 C25 MA_DQS_H2
MEM_MA_DQS_N2 D25 MA_DQS_L2
MEM_MA_DQS_P1 E19 MA_DQS_H1
MEM_MA_DQS_N1 F19 MA_DQS_L1
MEM_MA_DQS_P0 F15 MA_DQS_H0
MEM_MA_DQS_N0 G15 MA_DQS_L0

MEM_MA_DM7 AF15 MA_DM7
MEM_MA_DM6 AF19 MA_DM6
MEM_MA_DM5 AJ25 MA_DM5
MEM_MA_DM4 AH29 MA_DM4
MEM_MA_DM3 E24 MA_DM3
MEM_MA_DM2 E24 MA_DM2
MEM_MA_DM1 E18 MA_DM1
MEM_MA_DM0 H15 MA_DM0

MEM_MA_DQS_P7 AD15 MA_DQS_H7
MEM_MA_DQS_N7 AE15 MA_DQS_L7
MEM_MA_DQS_P6 AG18 MA_DQS_H6
MEM_MA_DQS_N6 AG19 MA_DQS_L6
MEM_MA_DQS_P5 AG24 MA_DQS_H5
MEM_MA_DQS_N5 AG25 MA_DQS_L5
MEM_MA_DQS_P4 AG27 MA_DQS_H4
MEM_MA_DQS_N4 AG28 MA_DQS_L4
MEM_MA_DQS_P3 AG28 MA_DQS_H3
MEM_MA_DQS_N3 C29 MA_DQS_L3
MEM_MA_DQS_P2 C25 MA_DQS_H2
MEM_MA_DQS_N2 D25 MA_DQS_L2
MEM_MA_DQS_P1 E19 MA_DQS_H1
MEM_MA_DQS_N1 F19 MA_DQS_L1
MEM_MA_DQS_P0 F15 MA_DQS_H0
MEM_MA_DQS_N0 G15 MA_DQS_L0

MEM_MA_DM7 AF15 MA_DM7
MEM_MA_DM6 AF19 MA_DM6
MEM_MA_DM5 AJ25 MA_DM5
MEM_MA_DM4 AH29 MA_DM4
MEM_MA_DM3 E24 MA_DM3
MEM_MA_DM2 E24 MA_DM2
MEM_MA_DM1 E18 MA_DM1
MEM_MA_DM0 H15 MA_DM0

MEM_MA_DQS_P7 AD15 MA_DQS_H7
MEM_MA_DQS_N7 AE15 MA_DQS_L7
MEM_MA_DQS_P6 AG18 MA_DQS_H6
MEM_MA_DQS_N6 AG19 MA_DQS_L6
MEM_MA_DQS_P5 AG24 MA_DQS_H5
MEM_MA_DQS_N5 AG25 MA_DQS_L5
MEM_MA_DQS_P4 AG27 MA_DQS_H4
MEM_MA_DQS_N4 AG28 MA_DQS_L4
MEM_MA_DQS_P3 AG28 MA_DQS_H3
MEM_MA_DQS_N3 C29 MA_DQS_L3
MEM_MA_DQS_P2 C25 MA_DQS_H2
MEM_MA_DQS_N2 D25 MA_DQS_L2
MEM_MA_DQS_P1 E19 MA_DQS_H1
MEM_MA_DQS_N1 F19 MA_DQS_L1
MEM_MA_DQS_P0 F15 MA_DQS_H0
MEM_MA_DQS_N0 G15 MA_DQS_L0

MEM_MA_DM7 AF15 MA_DM7
MEM_MA_DM6 AF19 MA_DM6
MEM_MA_DM5 AJ25 MA_DM5
MEM_MA_DM4 AH29 MA_DM4
MEM_MA_DM3 E24 MA_DM3
MEM_MA_DM2 E24 MA_DM2
MEM_MA_DM1 E18 MA_DM1
MEM_MA_DM0 H15 MA_DM0

MEM_MA_DQS_P7 AD15 MA_DQS_H7
MEM_MA_DQS_N7 AE15 MA_DQS_L7
MEM_MA_DQS_P6 AG18 MA_DQS_H6
MEM_MA_DQS_N6 AG19 MA_DQS_L6
MEM_MA_DQS_P5 AG24 MA_DQS_H5
MEM_MA_DQS_N5 AG25 MA_DQS_L5
MEM_MA_DQS_P4 AG27 MA_DQS_H4
MEM_MA_DQS_N4 AG28 MA_DQS_L4
MEM_MA_DQS_P3 AG28 MA_DQS_H3
MEM_MA_DQS_N3 C29 MA_DQS_L3
MEM_MA_DQS_P2 C25 MA_DQS_H2
MEM_MA_DQS_N2 D25 MA_DQS_L2
MEM_MA_DQS_P1 E19 MA_DQS_H1
MEM_MA_DQS_N1 F19 MA_DQS_L1
MEM_MA_DQS_P0 F15 MA_DQS_H0
MEM_MA_DQS_N0 G15 MA_DQS_L0

MEM_MA_DM7 AF15 MA_DM7
MEM_MA_DM6 AF19 MA_DM6
MEM_MA_DM5 AJ25 MA_DM5
MEM_MA_DM4 AH29 MA_DM4
MEM_MA_DM3 E24 MA_DM3
MEM_MA_DM2 E24 MA_DM2
MEM_MA_DM1 E18 MA_DM1
MEM_MA_DM0 H15 MA_DM0

MEM_MA_DQS_P7 AD15 MA_DQS_H7
MEM_MA_DQS_N7 AE15 MA_DQS_L7
MEM_MA_DQS_P6 AG18 MA_DQS_H6
MEM_MA_DQS_N6 AG19 MA_DQS_L6
MEM_MA_DQS_P5 AG24 MA_DQS_H5
MEM_MA_DQS_N5 AG25 MA_DQS_L5
MEM_MA_DQS_P4 AG27 MA_DQS_H4
MEM_MA_DQS_N4 AG28 MA_DQS_L4
MEM_MA_DQS_P3 AG28 MA_DQS_H3
MEM_MA_DQS_N3 C29 MA_DQS_L3
MEM_MA_DQS_P2 C25 MA_DQS_H2
MEM_MA_DQS_N2 D25 MA_DQS_L2
MEM_MA_DQS_P1 E19 MA_DQS_H1
MEM_MA_DQS_N1 F19 MA_DQS_L1
MEM_MA_DQS_P0 F15 MA_DQS_H0
MEM_MA_DQS_N0 G15 MA_DQS_L0

MEM_MA_DM7 AF15 MA_DM7
MEM_MA_DM6 AF19 MA_DM6
MEM_MA_DM5 AJ25 MA_DM5
MEM_MA_DM4 AH29 MA_DM4
MEM_MA_DM3 E24 MA_DM3
MEM_MA_DM2 E24 MA_DM2
MEM_MA_DM1 E18 MA_DM1
MEM_MA_DM0 H15 MA_DM0

MA_DATA63 AE14 MEM_MA_DATA63
MA_DATA62 AG14 MEM_MA_DATA62
MA_DATA61 AG16 MEM_MA_DATA61
MA_DATA60 AD17 MEM_MA_DATA60
MA_DATA59 AD13 MEM_MA_DATA59
MA_DATA58 AE13 MEM_MA_DATA58
MA_DATA57 AG15 MEM_MA_DATA57
MA_DATA56 AE16 MEM_MA_DATA56
MA_DATA55 AG17 MEM_MA_DATA55
MA_DATA54 AE18 MEM_MA_DATA54
MA_DATA53 AD21 MEM_MA_DATA53
MA_DATA52 AG22 MEM_MA_DATA52
MA_DATA51 AE17 MEM_MA_DATA51
MA_DATA50 AE17 MEM_MA_DATA50
MA_DATA49 AE21 MEM_MA_DATA49
MA_DATA48 AE21 MEM_MA_DATA48
MA_DATA47 AE23 MEM_MA_DATA47
MA_DATA46 AE23 MEM_MA_DATA46
MA_DATA45 AE23 MEM_MA_DATA45
MA_DATA44 AG26 MEM_MA_DATA44
MA_DATA43 AE22 MEM_MA_DATA43
MA_DATA42 AG24 MEM_MA_DATA42
MA_DATA41 AE25 MEM_MA_DATA41
MA_DATA40 AJ28 MEM_MA_DATA40
MA_DATA39 AE29 MEM_MA_DATA39
MA_DATA38 AE26 MEM_MA_DATA38
MA_DATA37 AE26 MEM_MA_DATA37
MA_DATA36 AE26 MEM_MA_DATA36
MA_DATA35 AE27 MEM_MA_DATA35
MA_DATA34 AE27 MEM_MA_DATA34
MA_DATA33 AE27 MEM_MA_DATA33
MA_DATA32 E29 MEM_MA_DATA32
MA_DATA31 E28 MEM_MA_DATA31
MA_DATA30 E27 MEM_MA_DATA30
MA_DATA29 E27 MEM_MA_DATA29
MA_DATA28 E27 MEM_MA_DATA28
MA_DATA27 E27 MEM_MA_DATA27
MA_DATA26 E27 MEM_MA_DATA26
MA_DATA25 E27 MEM_MA_DATA25
MA_DATA24 E27 MEM_MA_DATA24
MA_DATA23 E27 MEM_MA_DATA23
MA_DATA22 E27 MEM_MA_DATA22
MA_DATA21 E27 MEM_MA_DATA21
MA_DATA20 E27 MEM_MA_DATA20
MA_DATA19 E27 MEM_MA_DATA19
MA_DATA18 E27 MEM_MA_DATA18
MA_DATA17 E27 MEM_MA_DATA17
MA_DATA16 E27 MEM_MA_DATA16
MA_DATA15 E27 MEM_MA_DATA15
MA_DATA14 E27 MEM_MA_DATA14
MA_DATA13 E27 MEM_MA_DATA13
MA_DATA12 E27 MEM_MA_DATA12
MA_DATA11 E27 MEM_MA_DATA11
MA_DATA10 E27 MEM_MA_DATA10
MA_DATA9 E27 MEM_MA_DATA9
MA_DATA8 E27 MEM_MA_DATA8
MA_DATA7 E27 MEM_MA_DATA7
MA_DATA6 E27 MEM_MA_DATA6
MA_DATA5 E27 MEM_MA_DATA5
MA_DATA4 E27 MEM_MA_DATA4
MA_DATA3 E27 MEM_MA_DATA3
MA_DATA2 E27 MEM_MA_DATA2
MA_DATA1 E27 MEM_MA_DATA1
MA_DATA0 E27 MEM_MA_DATA0

MA0_CS_L1 AC25
MA0_CS_L0 AA24
MA0_ODT1 AE28
MA0_ODT0 AC28
MA1_CS_L1 AD27
MA1_CS_L0 AA25
MA1_ODT1 AE27
MA1_ODT0 AC27
MA_RESET_L TP37
MA_CAS_L AB25
MA_WE_L AB27
MA_RAS_L AA26
MA_BANK2 N25
MA_BANK1 Y27
MA_BANK0 AA27
MA_CKE1 L27
MA_CKE0 M25

MEM_MA_ADD15 M27
MEM_MA_ADD14 N24
MEM_MA_ADD13 AC26
MEM_MA_ADD12 N26
MEM_MA_ADD11 P25
MEM_MA_ADD10 Y25
MEM_MA_ADD9 N27
MEM_MA_ADD8 P24
MEM_MA_ADD7 P27
MEM_MA_ADD6 R25
MEM_MA_ADD5 R26
MEM_MA_ADD4 R27
MEM_MA_ADD3 T25
MEM_MA_ADD2 U25
MEM_MA_ADD1 T27
MEM_MA_ADD0 W24

MEM_MA_DQS_P7 AD15
MEM_MA_DQS_N7 AE15
MEM_MA_DQS_P6 AG18
MEM_MA_DQS_N6 AG19
MEM_MA_DQS_P5 AG24
MEM_MA_DQS_N5 AG25
MEM_MA_DQS_P4 AG27
MEM_MA_DQS_N4 AG28
MEM_MA_DQS_P3 AG28
MEM_MA_DQS_N3 C29
MEM_MA_DQS_P2 C25
MEM_MA_DQS_N2 D25
MEM_MA_DQS_P1 E19
MEM_MA_DQS_N1 F19
MEM_MA_DQS_P0 F15
MEM_MA_DQS_N0 G15

MEM_MA_DM7 AF15
MEM_MA_DM6 AF19
MEM_MA_DM5 AJ25
MEM_MA_DM4 AH29
MEM_MA_DM3 E24
MEM_MA_DM2 E24
MEM_MA_DM1 E18
MEM_MA_DM0 H15

MEM_MA_DQS_P7 AD15
MEM_MA_DQS_N7 AE15
MEM_MA_DQS_P6 AG18
MEM_MA_DQS_N6 AG19
MEM_MA_DQS_P5 AG24
MEM_MA_DQS_N5 AG25
MEM_MA_DQS_P4 AG27
MEM_MA_DQS_N4 AG28
MEM_MA_DQS_P3 AG28
MEM_MA_DQS_N3 C29
MEM_MA_DQS_P2 C25
MEM_MA_DQS_N2 D25
MEM_MA_DQS_P1 E19
MEM_MA_DQS_N1 F19
MEM_MA_DQS_P0 F15
MEM_MA_DQS_N0 G15

MEM_MA_DM7 AF15
MEM_MA_DM6 AF19
MEM_MA_DM5 AJ25
MEM_MA_DM4 AH29
MEM_MA_DM3 E24
MEM_MA_DM2 E24
MEM_MA_DM1 E18
MEM_MA_DM0 H15

MEM_MA_DQS_P7 AD15
MEM_MA_DQS_N7 AE15
MEM_MA_DQS_P6 AG18
MEM_MA_DQS_N6 AG19
MEM_MA_DQS_P5 AG24
MEM_MA_DQS_N5 AG25
MEM_MA_DQS_P4 AG27
MEM_MA_DQS_N4 AG28
MEM_MA_DQS_P3 AG28
MEM_MA_DQS_N3 C29
MEM_MA_DQS_P2 C25
MEM_MA_DQS_N2 D25
MEM_MA_DQS_P1 E19
MEM_MA_DQS_N1 F19
MEM_MA_DQS_P0 F15
MEM_MA_DQS_N0 G15

MEM_MA_DM7 AF15
MEM_MA_DM6 AF19
MEM_MA_DM5 AJ25
MEM_MA_DM4 AH29
MEM_MA_DM3 E24
MEM_MA_DM2 E24
MEM_MA_DM1 E18
MEM_MA_DM0 H15

ZIF-SOCKET941-RH

CPU1C

TP17 AJ19 MB_CLK_H7
TP19 AK19 MB_CLK_L7
TP18 AL19 MB_CLK_H6
TP20 AL18 MB_CLK_L6
U31 MB_CLK_L5
U30 MB_CLK_L4
W29 MB_CLK_H4
Y31 MB_CLK_L4
Y30 MB_CLK_H3
Y31 MB_CLK_L3
Y31 MB_CLK_H2
Y31 MB_CLK_L2
Y31 MB_CLK_H1
Y31 MB_CLK_L1
Y31 MB_CLK_H0
Y31 MB_CLK_L0

AE30 MB0_CS_L1
AC31 MB0_CS_L0
AF31 MB0_ODT1
AD29 MB0_ODT0
AE29 MB1_CS_L1
AB31 MB1_CS_L0
AG31 MB1_ODT1
AD31 MB1_ODT0
B19 MB_RESET_L

AC29 MB_CAS_L
AC30 MB_WE_L
AB29 MB_RAS_L
N31 MB_BANK2
A31 MB_BANK1
AA28 MB_BANK0
M31 MB_CKE1
M29 MB_CKE0

MEM_MB_ADD15 N28
MEM_MB_ADD14 N29
MEM_MB_ADD13 AE31
MEM_MB_ADD12 N30
MEM_MB_ADD11 P29
MEM_MB_ADD10 AA29
MEM_MB_ADD9 P31
MEM_MB_ADD8 R29
MEM_MB_ADD7 R28
MEM_MB_ADD6 R31
MEM_MB_ADD5 R30
MEM_MB_ADD4 T31
MEM_MB_ADD3 T29
MEM_MB_ADD2 U29
MEM_MB_ADD1 U28
MEM_MB_ADD0 AA30

MEM_MB_DQS_P7 AK13
MEM_MB_DQS_N7 AJ13
MEM_MB_DQS_P6 AK17
MEM_MB_DQS_N6 AJ17
MEM_MB_DQS_P5 AK23
MEM_MB_DQS_N5 AJ23
MEM_MB_DQS_P4 AL28
MEM_MB_DQS_N4 AL28
MEM_MB_DQS_P3 D31
MEM_MB_DQS_N3 C31
MEM_MB_DQS_P2 C24
MEM_MB_DQS_N2 C23
MEM_MB_DQS_P1 D17
MEM_MB_DQS_N1 C17
MEM_MB_DQS_P0 C14
MEM_MB_DQS_N0 C13

MEM_MB_DM7 AJ14
MEM_MB_DM6 AH17
MEM_MB_DM5 AJ23
MEM_MB_DM4 AK29
MEM_MB_DM3 C30
MEM_MB_DM2 A23
MEM_MB_DM1 B17
MEM_MB_DM0 B13

MEM_MB_ADD15 N28
MEM_MB_ADD14 N29
MEM_MB_ADD13 AE31
MEM_MB_ADD12 N30
MEM_MB_ADD11 P29
MEM_MB_ADD10 AA29
MEM_MB_ADD9 P31
MEM_MB_ADD8 R29
MEM_MB_ADD7 R28
MEM_MB_ADD6 R31
MEM_MB_ADD5 R30
MEM_MB_ADD4 T31
MEM_MB_ADD3 T29
MEM_MB_ADD2 U29
MEM_MB_ADD1 U28
MEM_MB_ADD0 AA30

MEM_MB_DQS_P7 AK13
MEM_MB_DQS_N7 AJ13
MEM_MB_DQS_P6 AK17
MEM_MB_DQS_N6 AJ17
MEM_MB_DQS_P5 AK23
MEM_MB_DQS_N5 AJ23
MEM_MB_DQS_P4 AL28
MEM_MB_DQS_N4 AL28
MEM_MB_DQS_P3 D31
MEM_MB_DQS_N3 C31
MEM_MB_DQS_P2 C24
MEM_MB_DQS_N2 C23
MEM_MB_DQS_P1 D17
MEM_MB_DQS_N1 C17
MEM_MB_DQS_P0 C14
MEM_MB_DQS_N0 C13

MEM_MB_DM7 AJ14
MEM_MB_DM6 AH17
MEM_MB_DM5 AJ23
MEM_MB_DM4 AK29
MEM_MB_DM3 C30
MEM_MB_DM2 A23
MEM_MB_DM1 B17
MEM_MB_DM0 B13

MEM_MB_ADD15 N28
MEM_MB_ADD14 N29
MEM_MB_ADD13 AE31
MEM_MB_ADD12 N30
MEM_MB_ADD11 P29
MEM_MB_ADD10 AA29
MEM_MB_ADD9 P31
MEM_MB_ADD8 R29
MEM_MB_ADD7 R28
MEM_MB_ADD6 R31
MEM_MB_ADD5 R30
MEM_MB_ADD4 T31
MEM_MB_ADD3 T29
MEM_MB_ADD2 U29
MEM_MB_ADD1 U28
MEM_MB_ADD0 AA30

MEM_MB_DQS_P7 AK13
MEM_MB_DQS_N7 AJ13
MEM_MB_DQS_P6 AK17
MEM_MB_DQS_N6 AJ17
MEM_MB_DQS_P5 AK23
MEM_MB_DQS_N5 AJ23
MEM_MB_DQS_P4 AL28
MEM_MB_DQS_N4 AL28
MEM_MB_DQS_P3 D31
MEM_MB_DQS_N3 C31
MEM_MB_DQS_P2 C24
MEM_MB_DQS_N2 C23
MEM_MB_DQS_P1 D17
MEM_MB_DQS_N1 C17
MEM_MB_DQS_P0 C14
MEM_MB_DQS_N0 C13

MEM_MB_DM7 AJ14
MEM_MB_DM6 AH17
MEM_MB_DM5 AJ23
MEM_MB_DM4 AK29
MEM_MB_DM3 C30
MEM_MB_DM2 A23
MEM_MB_DM1 B17
MEM_MB_DM0 B13

MEM_MB_ADD15 N28
MEM_MB_ADD14 N29
MEM_MB_ADD13 AE31
MEM_MB_ADD12 N30
MEM_MB_ADD11 P29
MEM_MB_ADD10 AA29
MEM_MB_ADD9 P31
MEM_MB_ADD8 R29
MEM_MB_ADD7 R28
MEM_MB_ADD6 R31
MEM_MB_ADD5 R30
MEM_MB_ADD4 T31
MEM_MB_ADD3 T29
MEM_MB_ADD2 U29
MEM_MB_ADD1 U28
MEM_MB_ADD0 AA30

MEM_MB_DQS_P7 AK13
MEM_MB_DQS_N7 AJ13
MEM_MB_DQS_P6 AK17
MEM_MB_DQS_N6 AJ17
MEM_MB_DQS_P5 AK23
MEM_MB_DQS_N5 AJ23
MEM_MB_DQS_P4 AL28
MEM_MB_DQS_N4 AL28
MEM_MB_DQS_P3 D31
MEM_MB_DQS_N3 C31
MEM_MB_DQS_P2 C24
MEM_MB_DQS_N2 C23
MEM_MB_DQS_P1 D17
MEM_MB_DQS_N1 C17
MEM_MB_DQS_P0 C14
MEM_MB_DQS_N0 C13

MEM_MB_DM7 AJ14
MEM_MB_DM6 AH17
MEM_MB_DM5 AJ23
MEM_MB_DM4 AK29
MEM_MB_DM3 C30
MEM_MB_DM2 A23
MEM_MB_DM1 B17
MEM_MB_DM0 B13

MEM CHB

MB_CLK_H7 MB_DATA63
MB_CLK_L7 MB_DATA62
MB_CLK_H6 MB_DATA61
MB_CLK_L6 MB_DATA60
MB_CLK_L5 MB_DATA59
MB_CLK_L4 MB_DATA58
MB_CLK_H4 MB_DATA57
MB_CLK_L4 MB_DATA56
MB_CLK_H3 MB_DATA55
MB_CLK_L3 MB_DATA54
MB_CLK_H2 MB_DATA53
MB_CLK_L2 MB_DATA52
MB_CLK_H1 MB_DATA51
MB_CLK_L1 MB_DATA50
MB_CLK_H0 MB_DATA49
MB_CLK_L0 MB_DATA48

MB0_CS_L1 MB0_CS_L0
MB0_ODT1 MB0_ODT0
MB1_CS_L1 MB1_CS_L0
MB1_ODT1 MB1_ODT0
MB_RESET_L

MB_CAS_L MB_WE_L
MB_RAS_L MB_BANK2
MB_BANK1 MB_BANK0
MB_CKE1 MB_CKE0

MEM_MB_ADD15 N28
MEM_MB_ADD14 N29
MEM_MB_ADD13 AE31
MEM_MB_ADD12 N30
MEM_MB_ADD11 P29
MEM_MB_ADD10 AA29
MEM_MB_ADD9 P31
MEM_MB_ADD8 R29
MEM_MB_ADD7 R28
MEM_MB_ADD6 R31
MEM_MB_ADD5 R30
MEM_MB_ADD4 T31
MEM_MB_ADD3 T29
MEM_MB_ADD2 U29
MEM_MB_ADD1 U28
MEM_MB_ADD0 AA30

MEM_MB_DQS_P7 AK13
MEM_MB_DQS_N7 AJ13
MEM_MB_DQS_P6 AK17
MEM_MB_DQS_N6 AJ17
MEM_MB_DQS_P5 AK23
MEM_MB_DQS_N5 AJ23
MEM_MB_DQS_P4 AL28
MEM_MB_DQS_N4 AL28
MEM_MB_DQS_P3 D31
MEM_MB_DQS_N3 C31
MEM_MB_DQS_P2 C24
MEM_MB_DQS_N2 C23
MEM_MB_DQS_P1 D17
MEM_MB_DQS_N1 C17
MEM_MB_DQS_P0 C14
MEM_MB_DQS_N0 C13

MEM_MB_DM7 AJ14
MEM_MB_DM6 AH17
MEM_MB_DM5 AJ23
MEM_MB_DM4 AK29
MEM_MB_DM3 C30
MEM_MB_DM2 A23
MEM_MB_DM1 B17
MEM_MB_DM0 B13

MEM_MB_ADD15 N28
MEM_MB_ADD14 N29
MEM_MB_ADD13 AE31
MEM_MB_ADD12 N30
MEM_MB_ADD11 P29
MEM_MB_ADD10 AA29
MEM_MB_ADD9 P31
MEM_MB_ADD8 R29
MEM_MB_ADD7 R28
MEM_MB_ADD6 R31
MEM_MB_ADD5 R30
MEM_MB_ADD4 T31
MEM_MB_ADD3 T29
MEM_MB_ADD2 U29
MEM_MB_ADD1 U28
MEM_MB_ADD0 AA30

MEM_MB_DQS_P7 AK13
MEM_MB_DQS_N7 AJ13
MEM_MB_DQS_P6 AK17
MEM_MB_DQS_N6 AJ17
MEM_MB_DQS_P5 AK23
MEM_MB_DQS_N5 AJ23
MEM_MB_DQS_P4 AL28
MEM_MB_DQS_N4 AL28
MEM_MB_DQS_P3 D31
MEM_MB_DQS_N3 C31
MEM_MB_DQS_P2 C24
MEM_MB_DQS_N2 C23
MEM_MB_DQS_P1 D17
MEM_MB_DQS_N1 C17
MEM_MB_DQS_P0 C14
MEM_MB_DQS_N0 C13

MEM_MB_DM7 AJ14
MEM_MB_DM6 AH17
MEM_MB_DM5 AJ23
MEM_MB_DM4 AK29
MEM_MB_DM3 C30
MEM_MB_DM2 A23
MEM_MB_DM1 B17
MEM_MB_DM0 B13

MEM_MB_ADD15 N28
MEM_MB_ADD14 N29
MEM_MB_ADD13 AE31
MEM_MB_ADD12 N30
MEM_MB_ADD11 P29
MEM_MB_ADD10 AA29
MEM_MB_ADD9 P31
MEM_MB_ADD8 R29
MEM_MB_ADD7 R28
MEM_MB_ADD6 R31
MEM_MB_ADD5 R30
MEM_MB_ADD4 T31
MEM_MB_ADD3 T29
MEM_MB_ADD2 U29
MEM_MB_ADD1 U28
MEM_MB_ADD0 AA30

MEM_MB_DQS_P7 AK13
MEM_MB_DQS_N7 AJ13
MEM_MB_DQS_P6 AK17
MEM_MB_DQS_N6 AJ17
MEM_MB_DQS_P5 AK23
MEM_MB_DQS_N5 AJ23
MEM_MB_DQS_P4 AL28
MEM_MB_DQS_N4 AL28
MEM_MB_DQS_P3 D31
MEM_MB_DQS_N3 C31
MEM_MB_DQS_P2 C24
MEM_MB_DQS_N2 C23
MEM_MB_DQS_P1 D17
MEM_MB_DQS_N1 C17
MEM_MB_DQS_P0 C14
MEM_MB_DQS_N0 C13

MEM_MB_DM7 AJ14
MEM_MB_DM6 AH17
MEM_MB_DM5 AJ23
MEM_MB_DM4 AK29
MEM_MB_DM3 C30
MEM_MB_DM2 A23
MEM_MB_DM1 B17
MEM_MB_DM0 B13

MEM_MB_ADD15 N28
MEM_MB_ADD14 N29
MEM_MB_ADD13 AE31
MEM_MB_ADD12 N30
MEM_MB_ADD11 P29
MEM_MB_ADD10 AA29
MEM_MB_ADD9 P31
MEM_MB_ADD8 R29
MEM_MB_ADD7 R28
MEM_MB_ADD6 R31
MEM_MB_ADD5 R30
MEM_MB_ADD4 T31
MEM_MB_ADD3 T29
MEM_MB_ADD2 U29
MEM_MB_ADD1 U28
MEM_MB_ADD0 AA30

MEM_MB_DQS_P7 AK13
MEM_MB_DQS_N7 AJ13
MEM_MB_DQS_P6 AK17
MEM_MB_DQS_N6 AJ17
MEM_MB_DQS_P5 AK23
MEM_MB_DQS_N5 AJ23
MEM_MB_DQS_P4 AL28
MEM_MB_DQS_N4 AL28
MEM_MB_DQS_P3 D31
MEM_MB_DQS_N3 C31
MEM_MB_DQS_P2 C24
MEM_MB_DQS_N2 C23
MEM_MB_DQS_P1 D17
MEM_MB_DQS_N1 C17
MEM_MB_DQS_P0 C14
MEM_MB_DQS_N0 C13

MEM_MB_DM7 AJ14
MEM_MB_DM6 AH17
MEM_MB_DM5 AJ23
MEM_MB_DM4 AK29
MEM_MB_DM3 C30
MEM_MB_DM2 A23
MEM_MB_DM1 B17
MEM_MB_DM0 B13

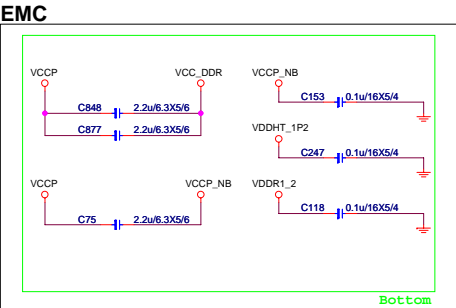
ZIF-SOCKET941-RH

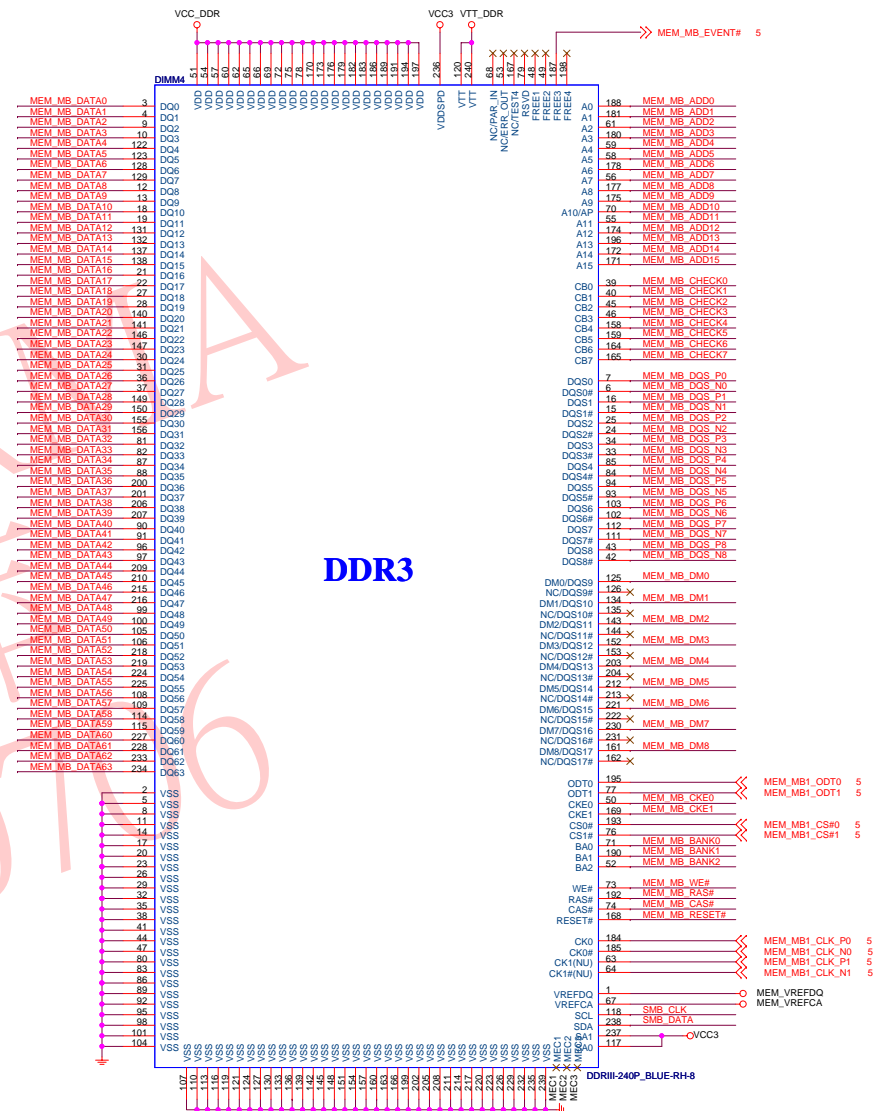


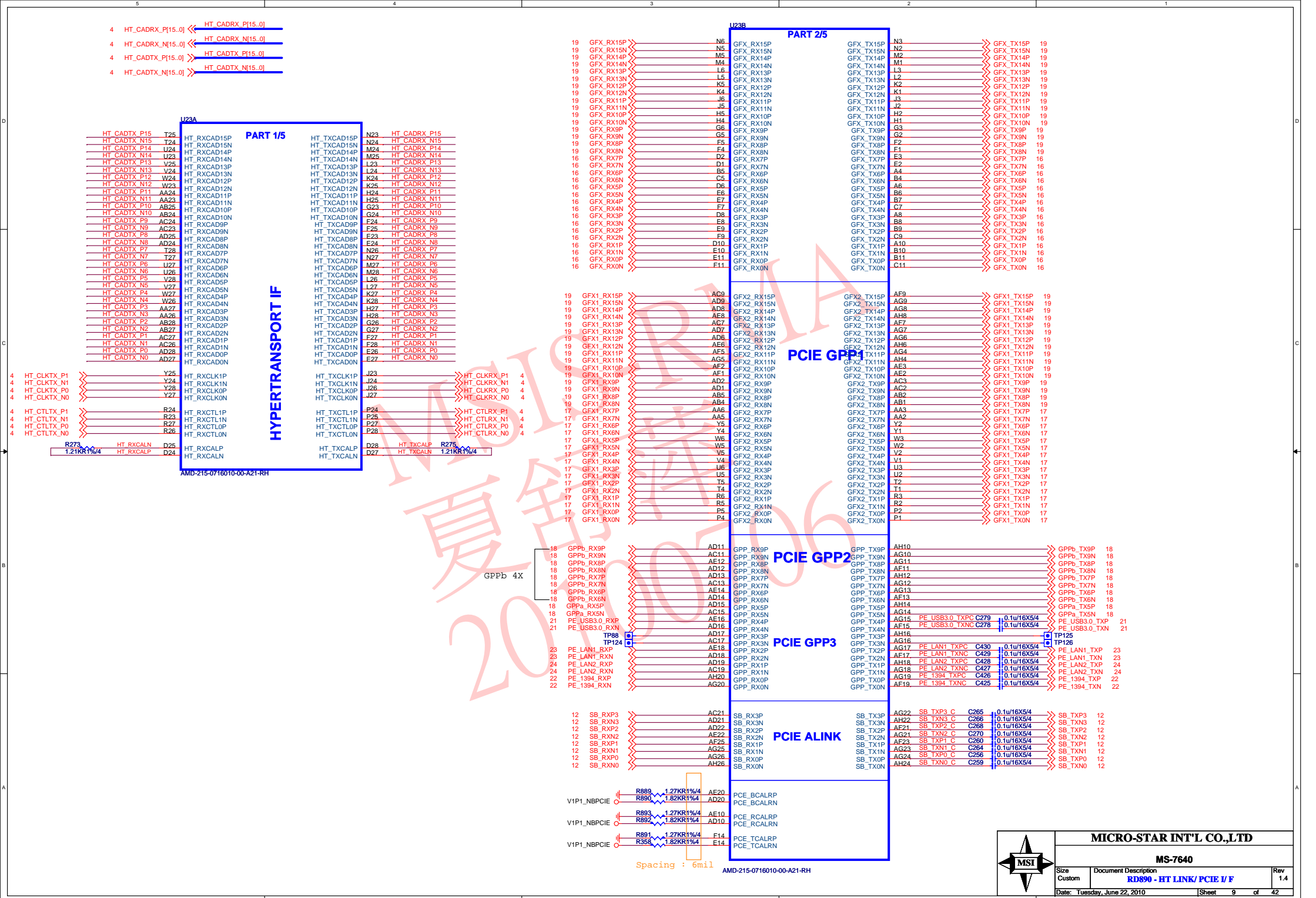
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Size Custom Document Description K9 AM3 - CPU MEMORY Rev 1.4
Date: Tuesday, June 22, 2010 Sheet 5 of 42







DFT_GPIO5: STRAP_DEBUG_BUS_GPIO_ENABLED

Enables the Test Debug Bus using GPIO.
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.
GPIO4:3:2

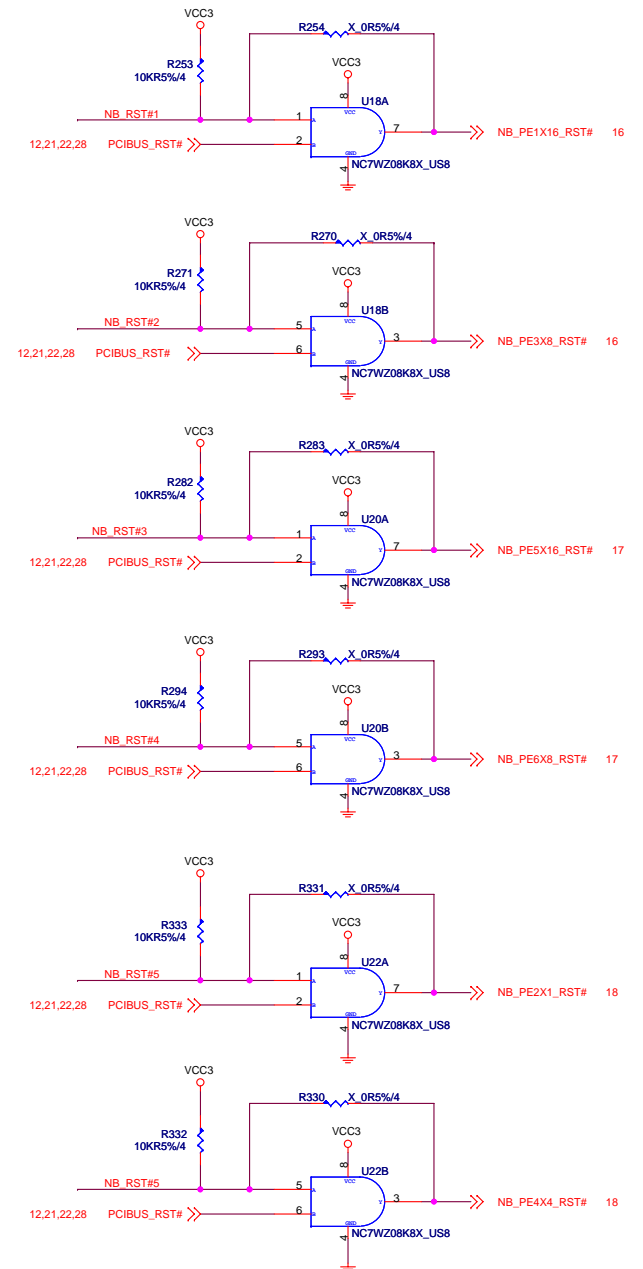
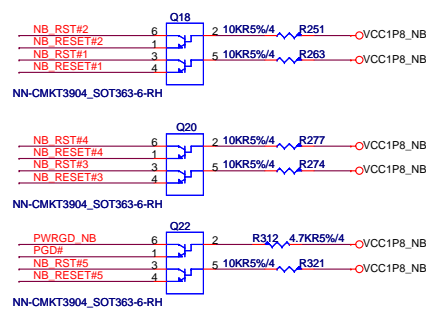
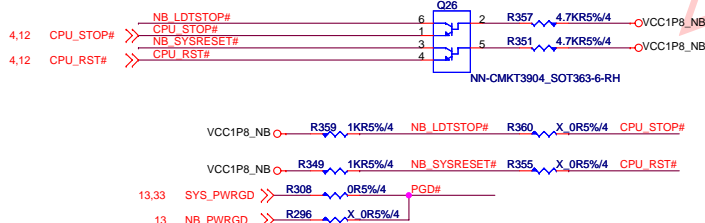
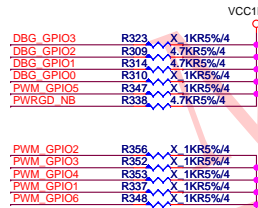
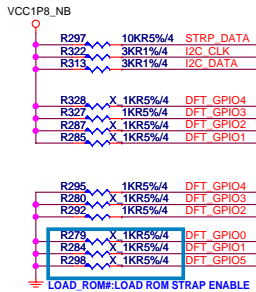
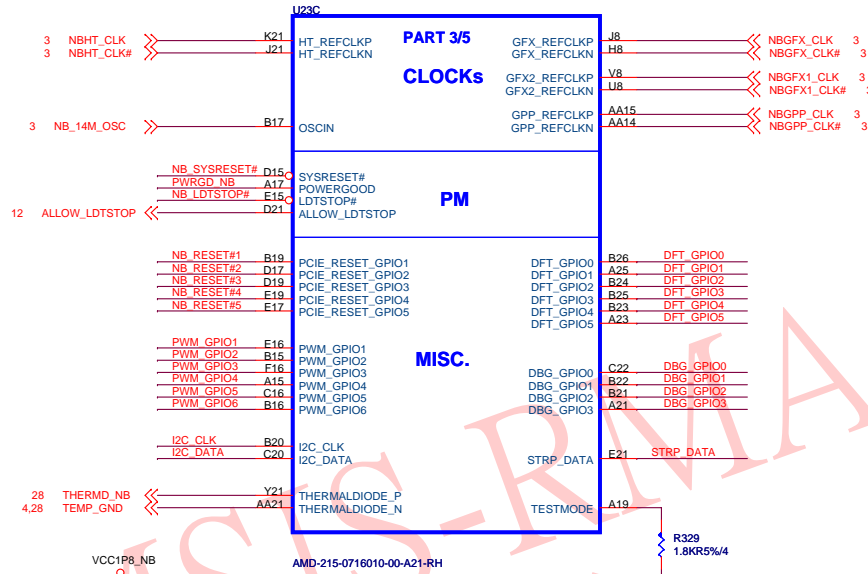
010 : 1:1:1:1:1:1:4 L

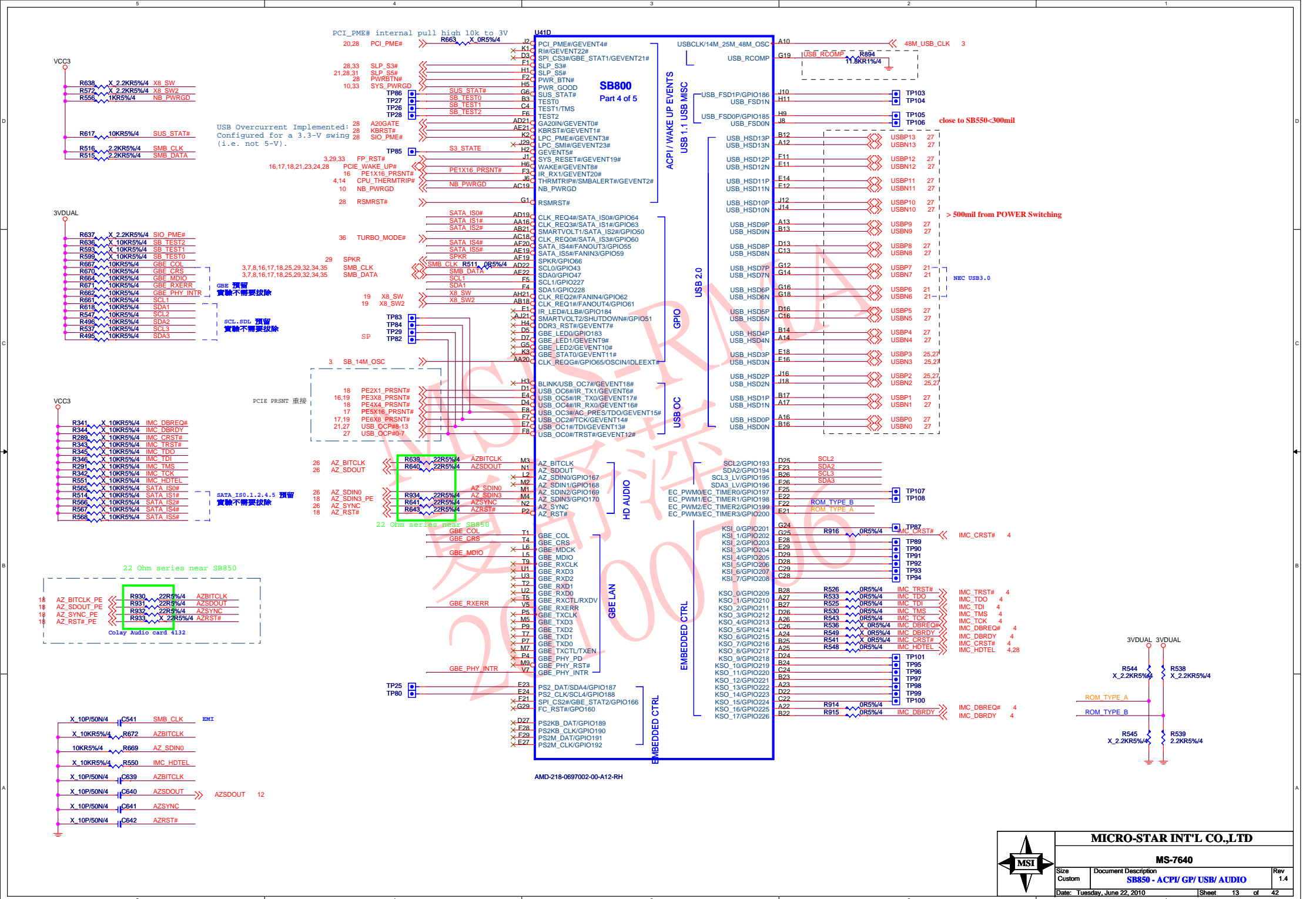
DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EPROM if connected, or use default values if not connected

DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLED

Enables the Test Debug Bus using PCIE bus
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable



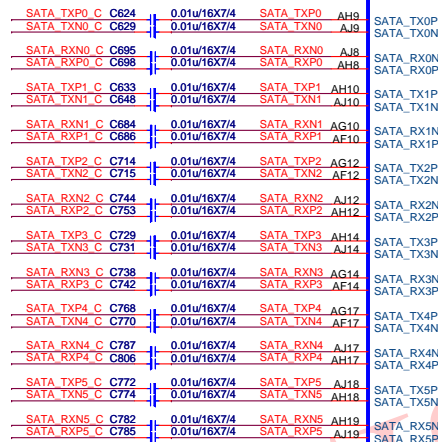


MICRO-STAR INT'L CO.,LTD

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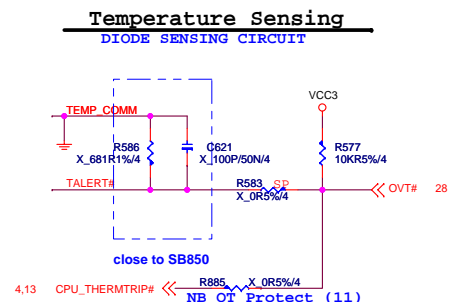
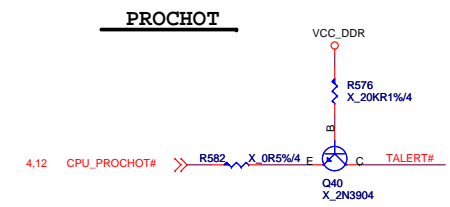
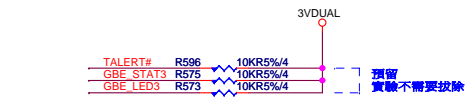
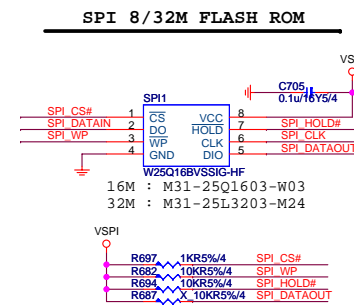
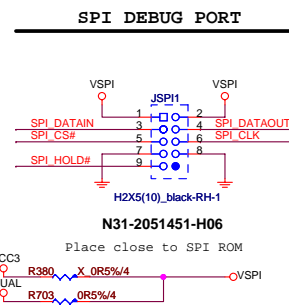
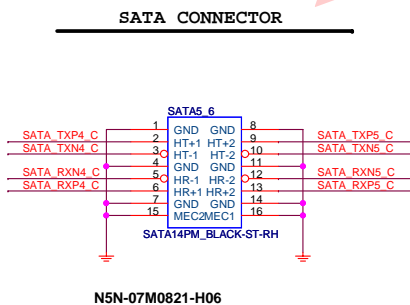
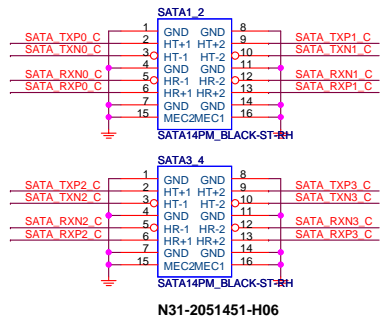
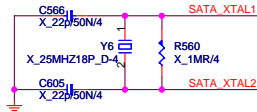
Size Custom	Document Description SB850 - ACPI/ GP/ USB/ AUDIO	Rev 1.4
Date: Tuesday, June 22, 2010		Sheet 13 of 42

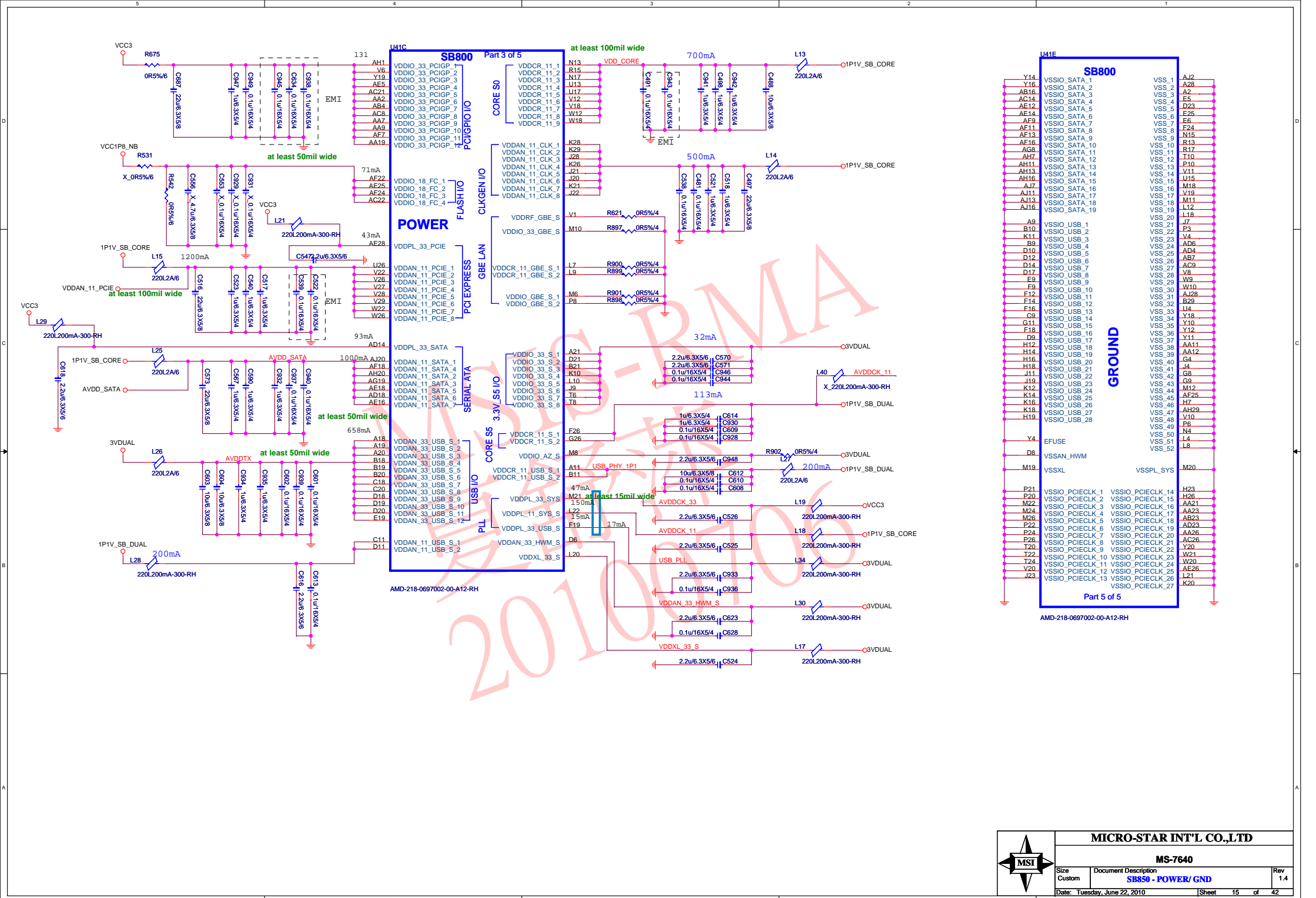
Place AC coupling caps close to
SATA connector
Place AC coupling caps close to SB550 (CRB)



AVDD_SATA
SATA_LED#
SATA_XTAL1
SATA_XTAL2

1K 1% for XTAL,
4.99K 1% for 100M INTERNAL CLK



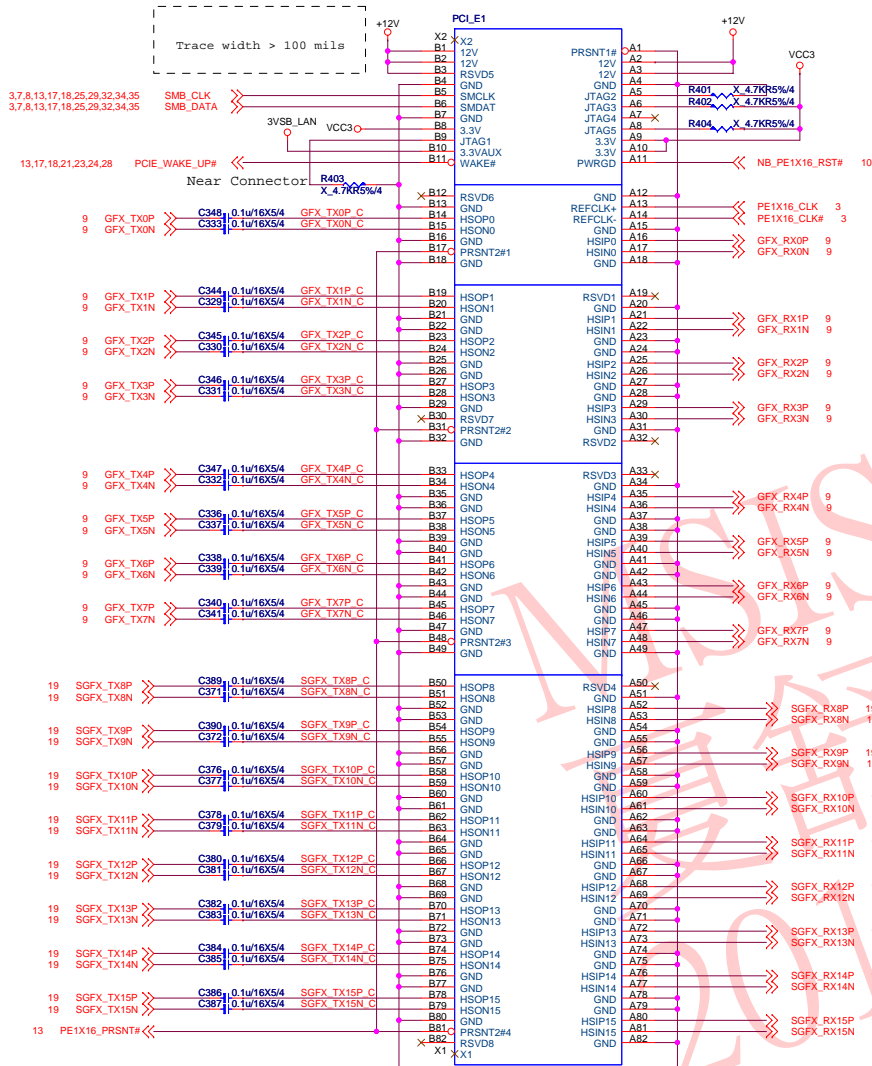


MICRO-STAR INT'L CO.,LTD

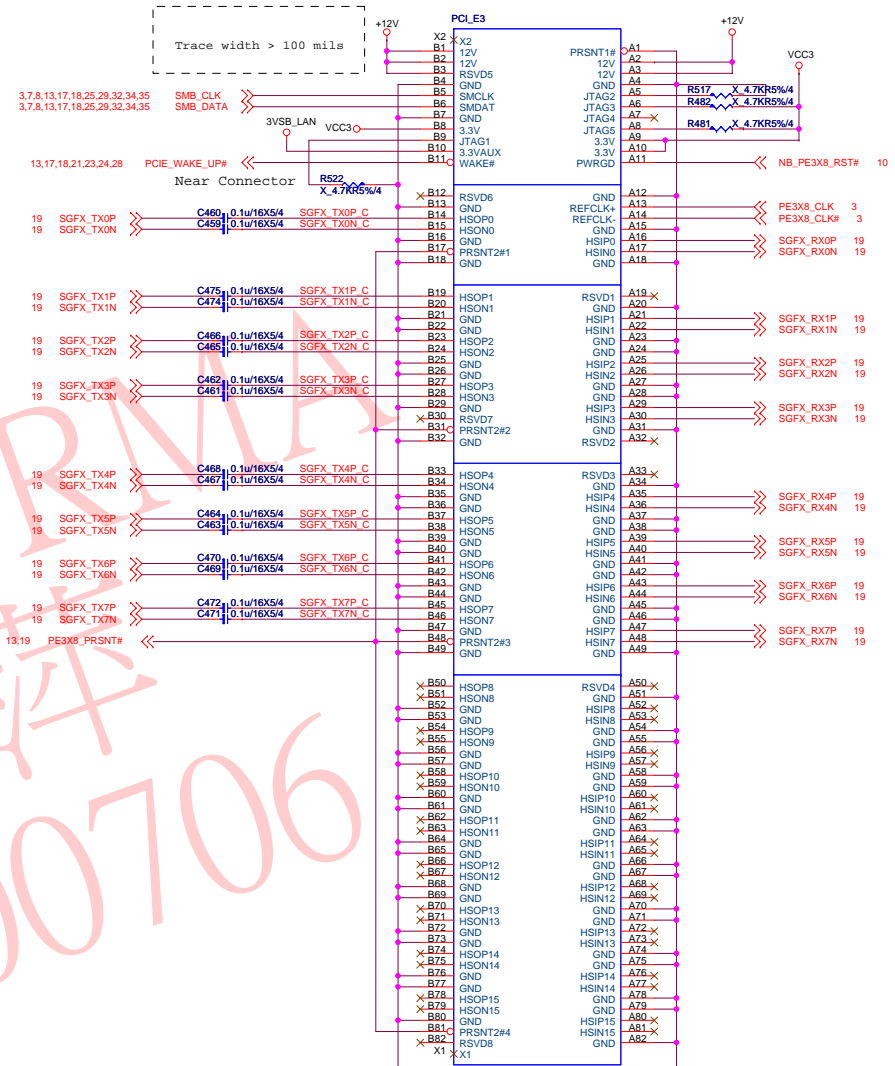
MS-7640

Size Custom	Document Description SB850 - POWER/ GND	Rev 1.4
Date: Tuesday, June 22, 2010		Sheet 15 of 42

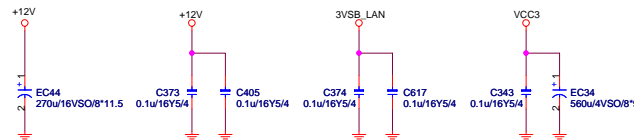
PCI-EXPRESS X16



SLOT-PCI164P_BLUE-2PITCH-RH-3
N11-1640711-L06, blue

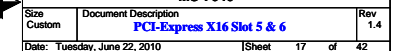


SLOT-PCI164P_BLUE-2PITCH-RH-3
N11-1640711-L06, blue

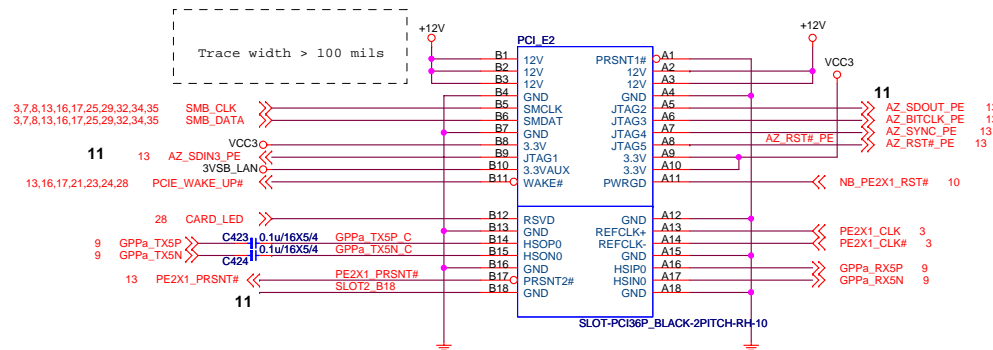


記得在SLOT旁接電容

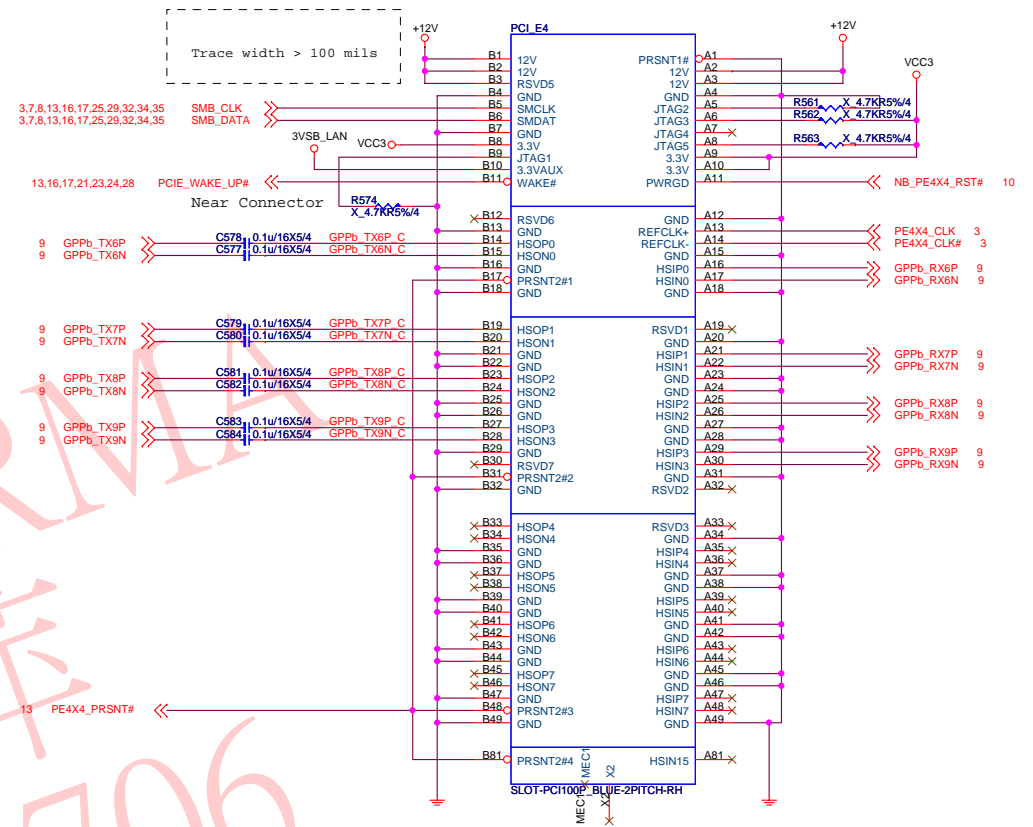
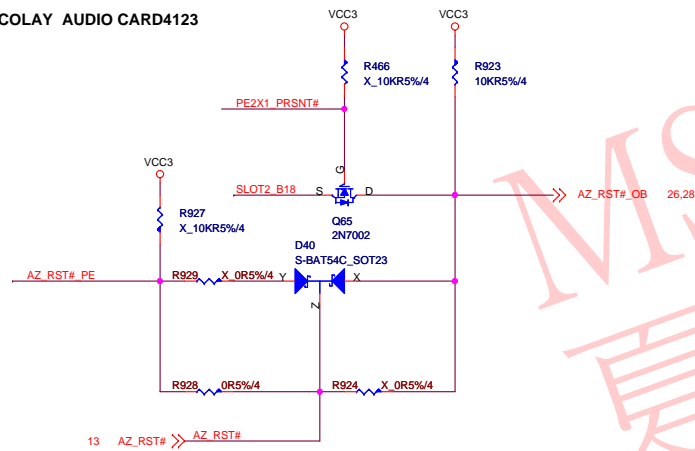
N11-1640711-L06, blue



PCI-EXPRESS X16

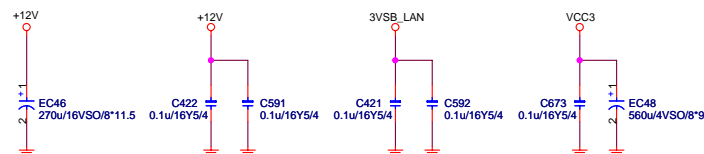


N11-0360281-K06



N11-1000011-L06, Blue (11)

	B17	B18	AZ_RST#_OB	AZ_RST#_PE
N/C	HIGH	N/C	HIGH	HIGH
PEIC X1	GND	GND	HIGH	HIGH
Audio card(4132)	HIGH	GND	LOW	HIGH

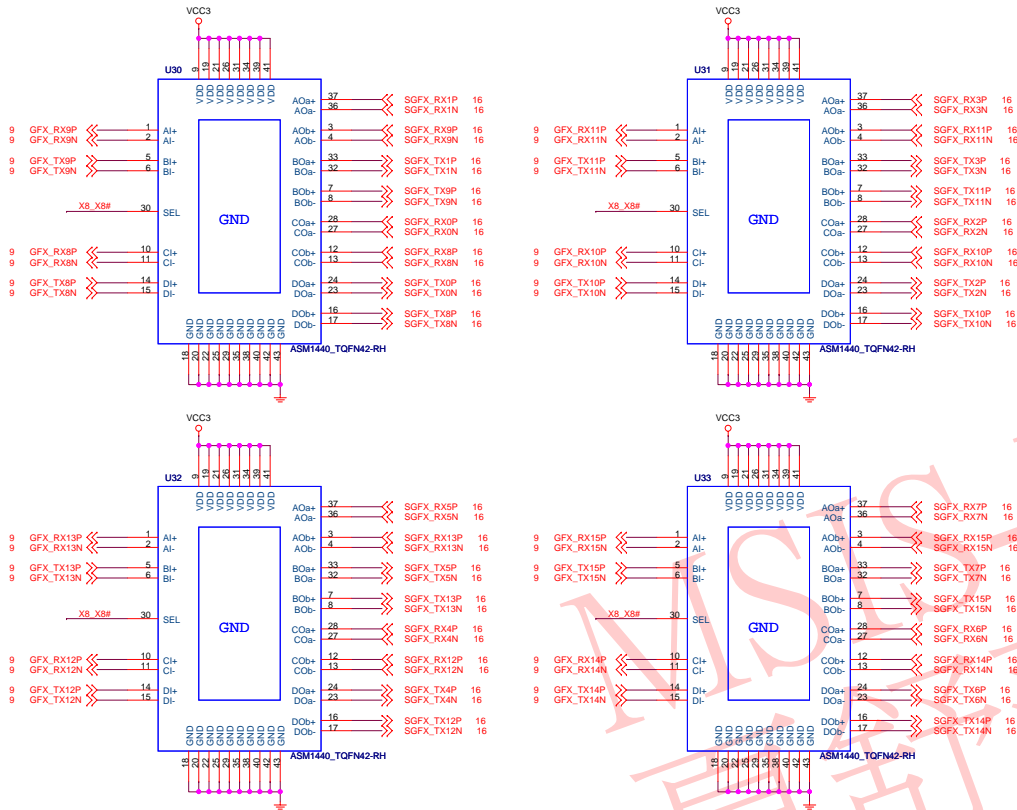


MICRO-STAR INT'L CO.,LTD

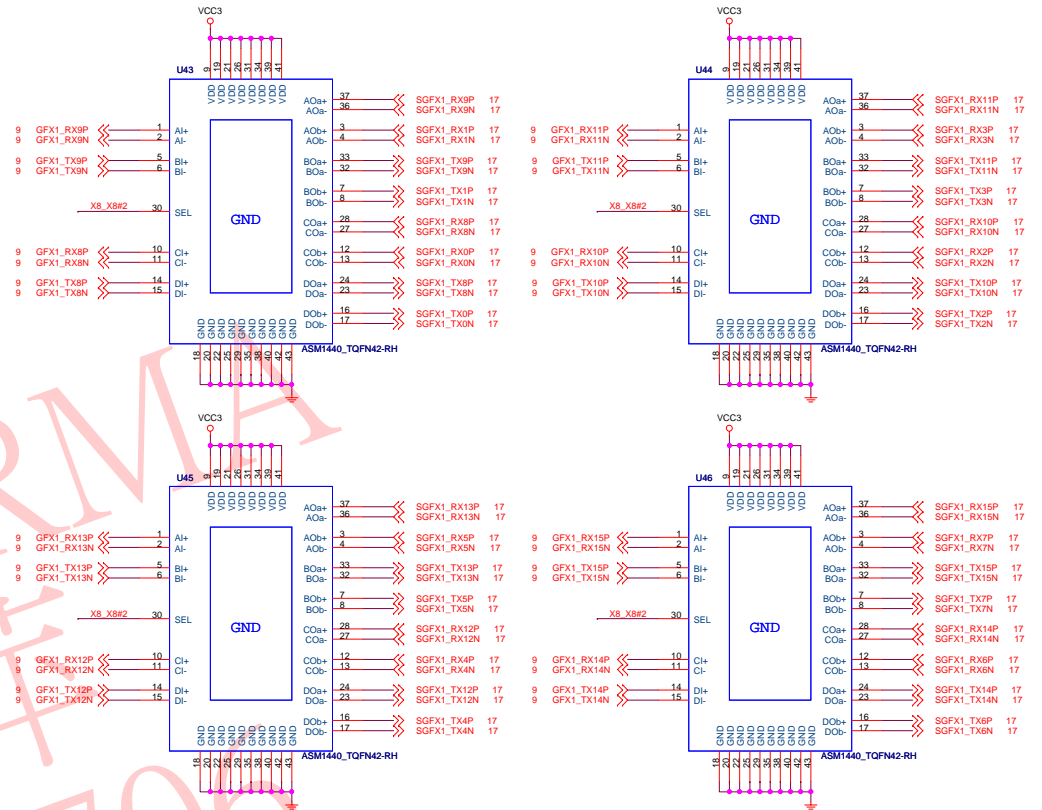
MS-7640

Size Custom	Document Description PCI-Express X4 Slot 2 & 4	Rev 1.4
Date: Tuesday, June 22, 2010		Sheet 18 of 42

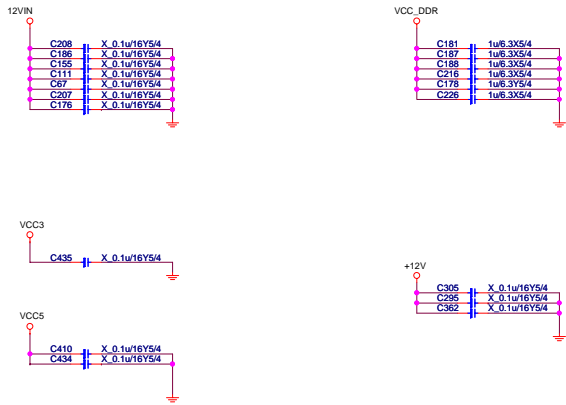
PCI-E SLOT 3 & 6 Switching



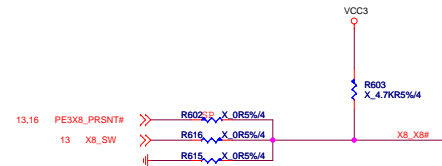
PCI-E SLOT 5 & 6 Switching



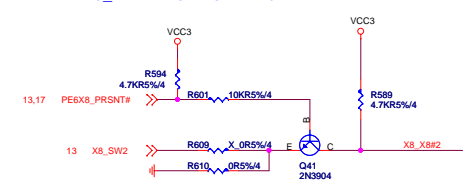
EMI



X8_SW hi for X16



X8_SW low for X16



MICRO-STAR INT'L CO., LTD.

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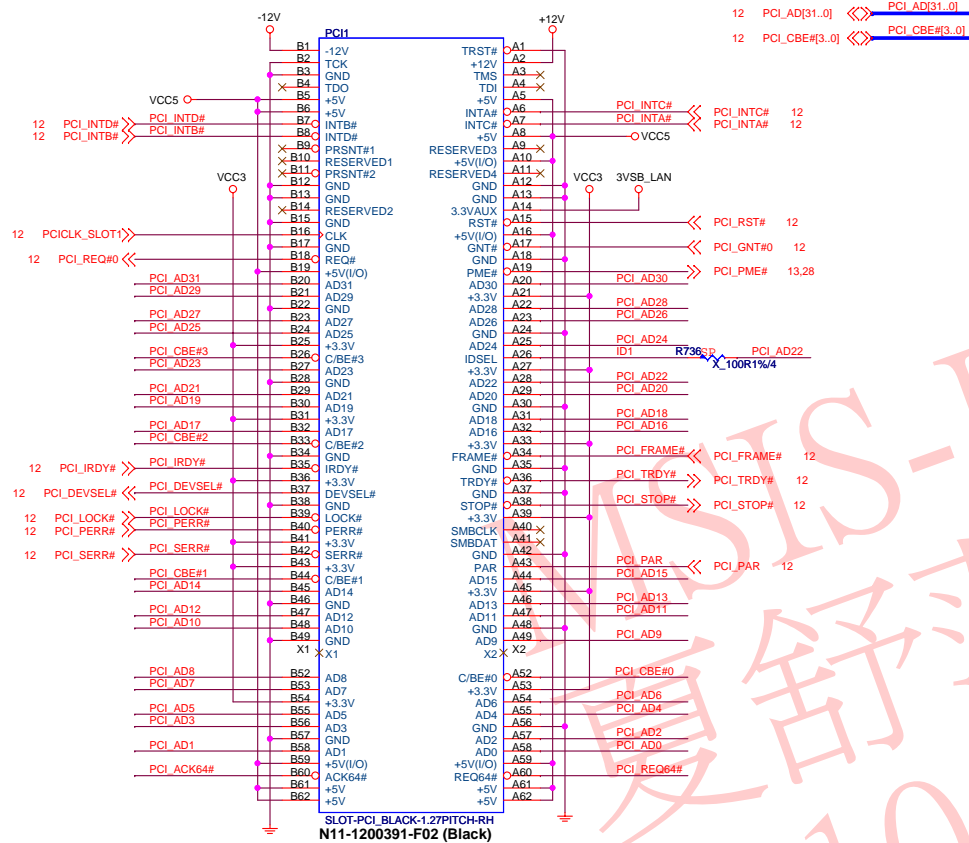
Size Custom Document Description

PCI-Express Slot 2/4 SW

Rev 1.4

Date: Tuesday, June 22, 2010 Sheet 19 of 42

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



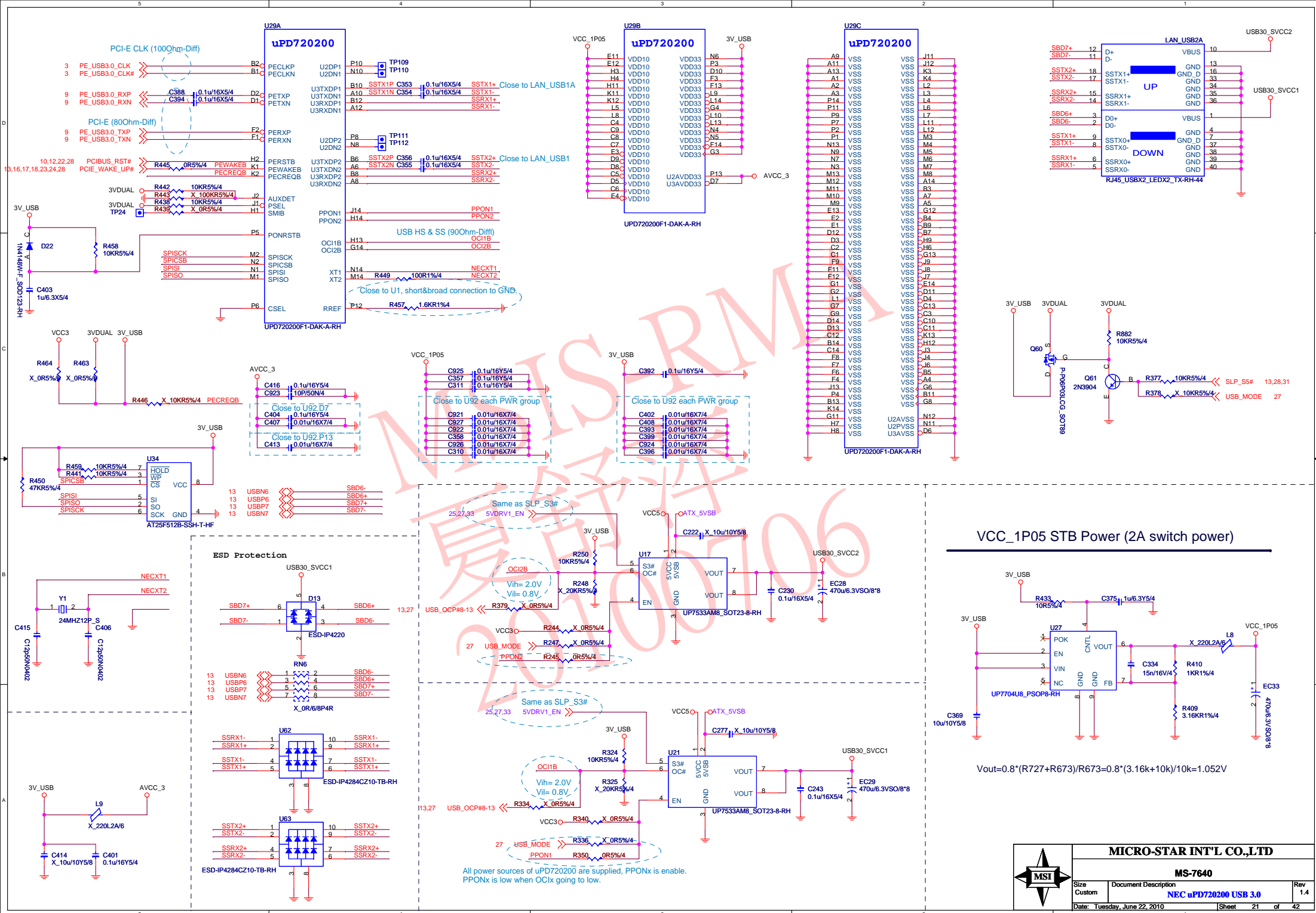
SLOT-PCI_BLACK-1.27PITCH-RH
N11-1200391-F02 (Black)

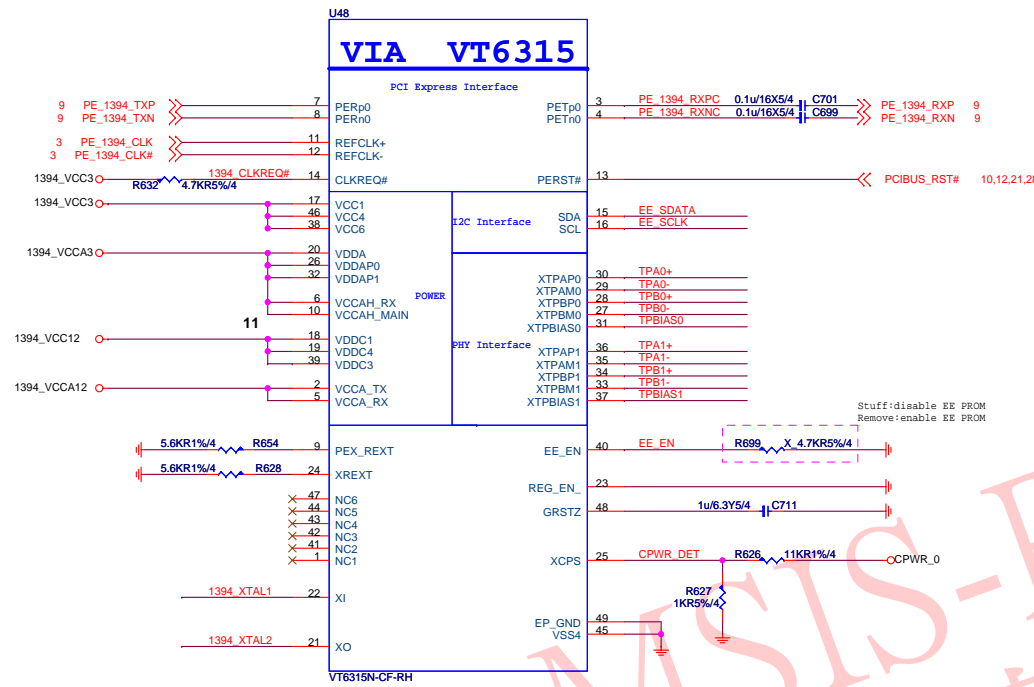
IDSEL = AD22

MASTER = PCI_REQ#0

PCI_GNT#0

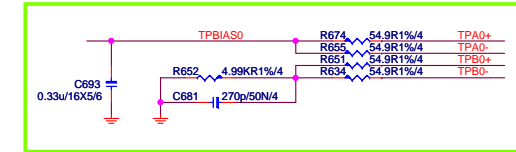
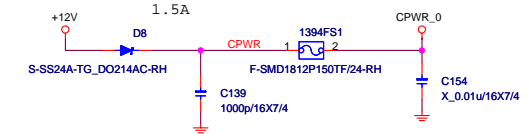




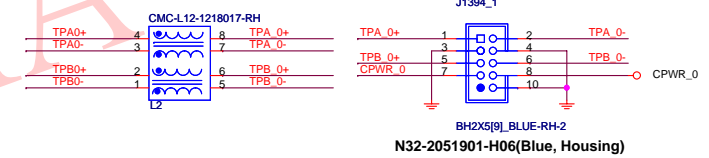


Rear 1394 port

60 mils

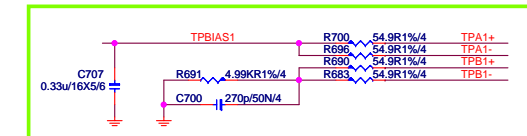
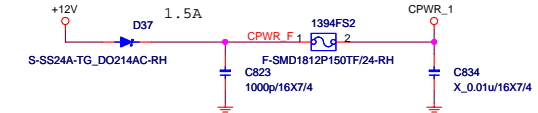


Close to IC

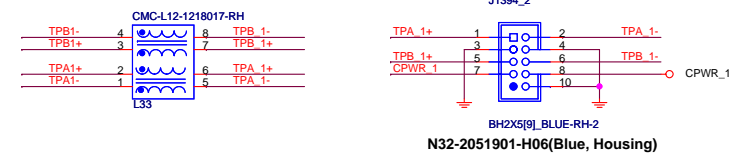


Front 1394

60 mils



Close to IC

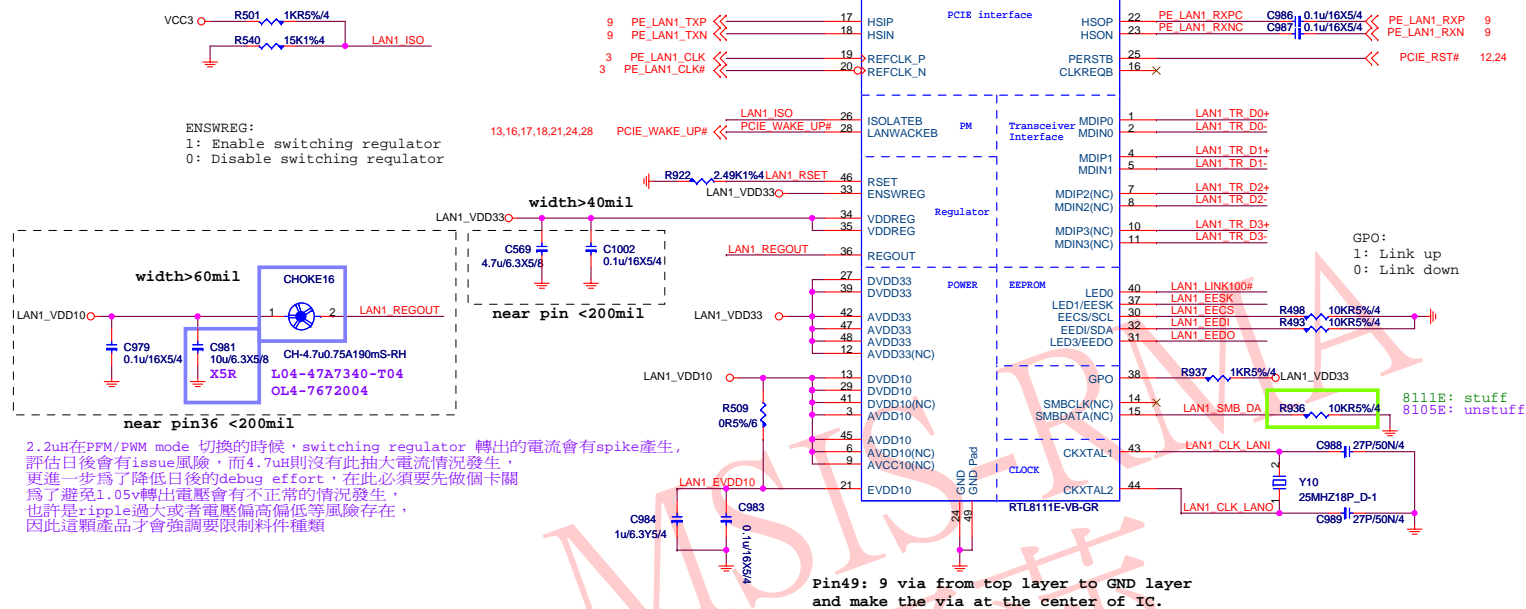


For Intel 1394 pinheader

All 0.1u cap near to IC power pin

MICRO-STAR INT'L CO.,LTD			
MS-7640			
Size	Document Description		Rev
Custom	1394 Controller - VIA VT6315N		1.4
Date:	Tuesday, June 22, 2010	Sheet	22 of 42

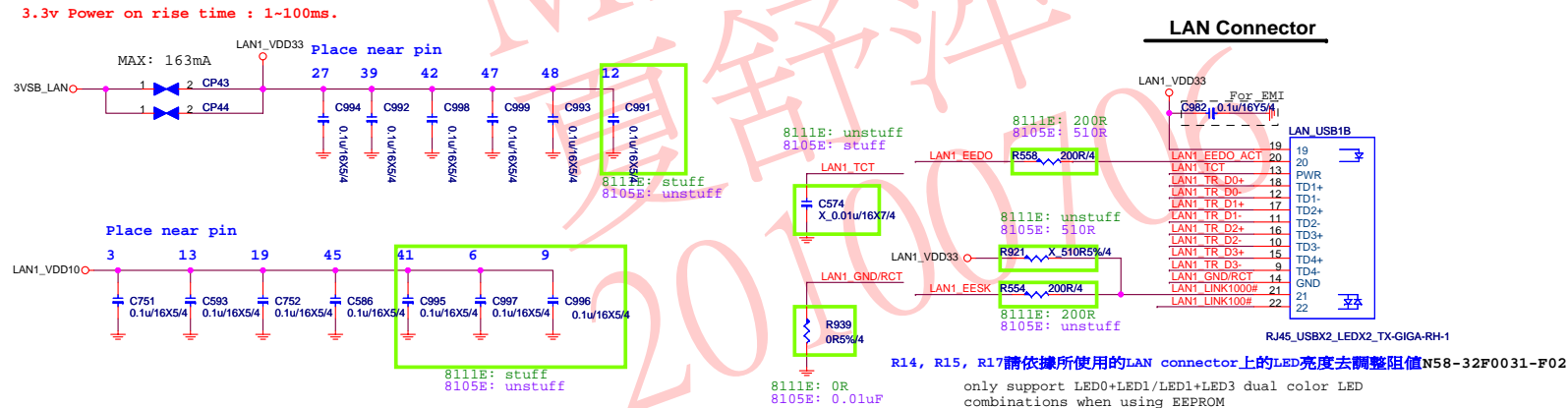
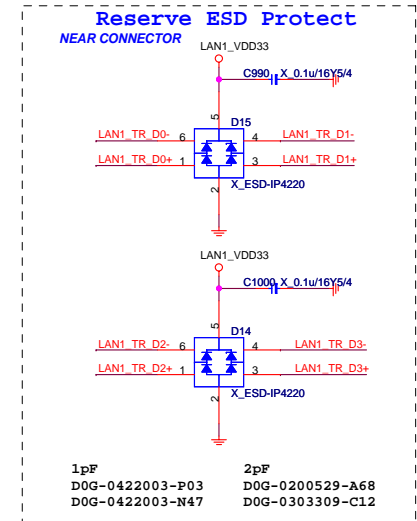
```
RTL8111E Giga LAN
RTL8105E 10/100M LAN
```



LAN1_VDD33

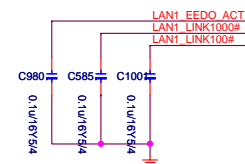
PCIE_WAKE_UP# R492 X 10KR5%4




Remove pull-up R if R existence on motherboard (or SB has internal pull-up R).



8105E POWER Consumption		
	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11

8111E POWER Consumption		
	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13



Giga-Lan		10/100-Lan	
N58-22F0081-S42		N58-22F0061-S42 N58-22F0061-F02	
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	100	Green
100	Green	10	None
10	None		
19		19	
20	Yellow	20	Yellow
21	Orange	21	
22	Green	22	Green

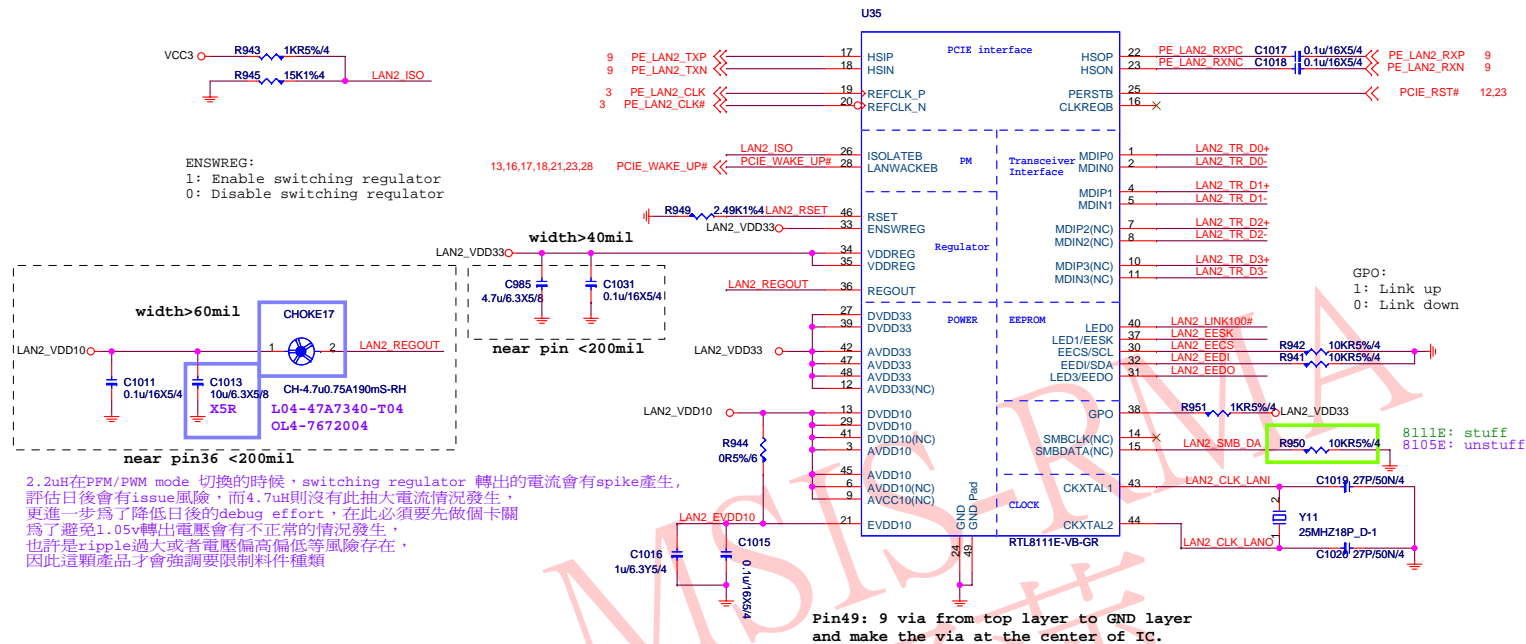


MICRO-STAR INT'L CO.,LTD

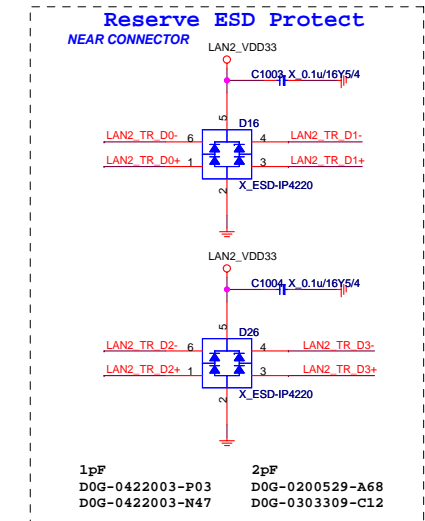
MS-7640

Size Custom	Document Description LANI RTL 8111E	Rev 1.4
Date: Tuesday, June 22, 2010		Sheet 23 of 42

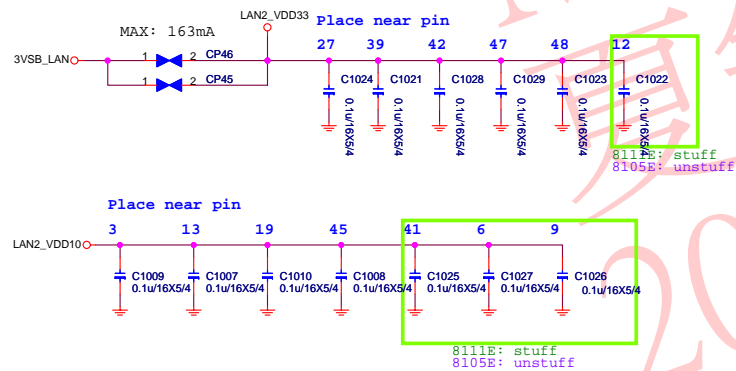
RTL8105E 10/100M LAN



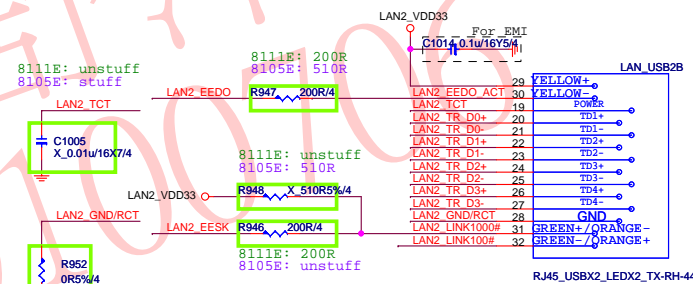
Remove pull-up R if R existence on motherboard (or SB has internal pull-up R).



3.3v Power on rise time : 1~100ms.



LAN Connector



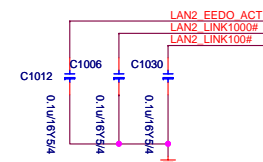
R14, R15, R17請依據所使用的LAN connector上的LED亮度去調整阻值N58-32F0031-F02
only support LED0+LED1/LED1+LED3 dual color LED
combinations when using EEPROM



8105E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11

8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13



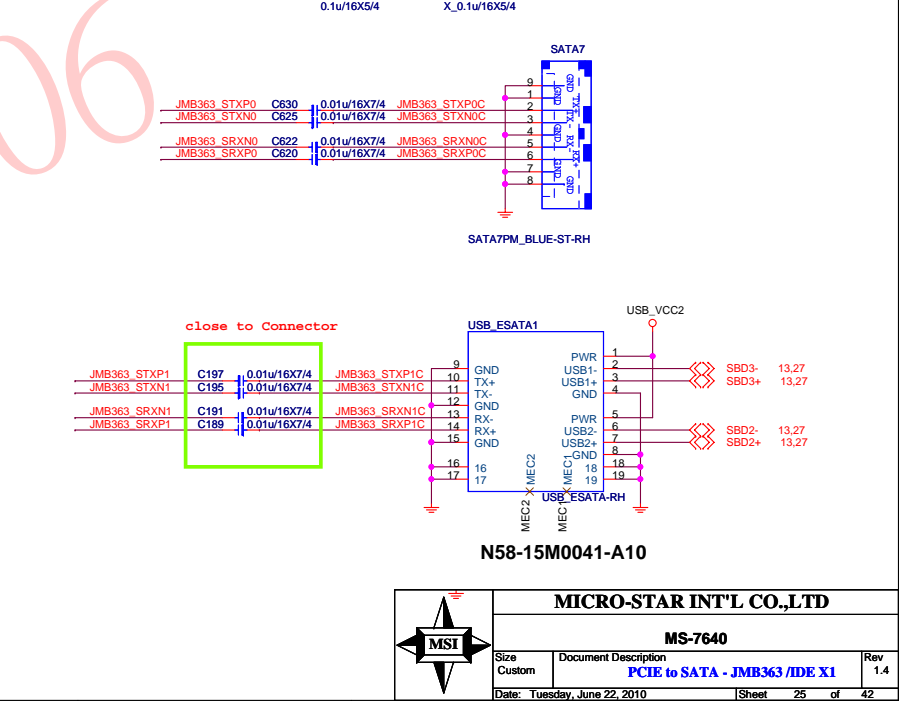
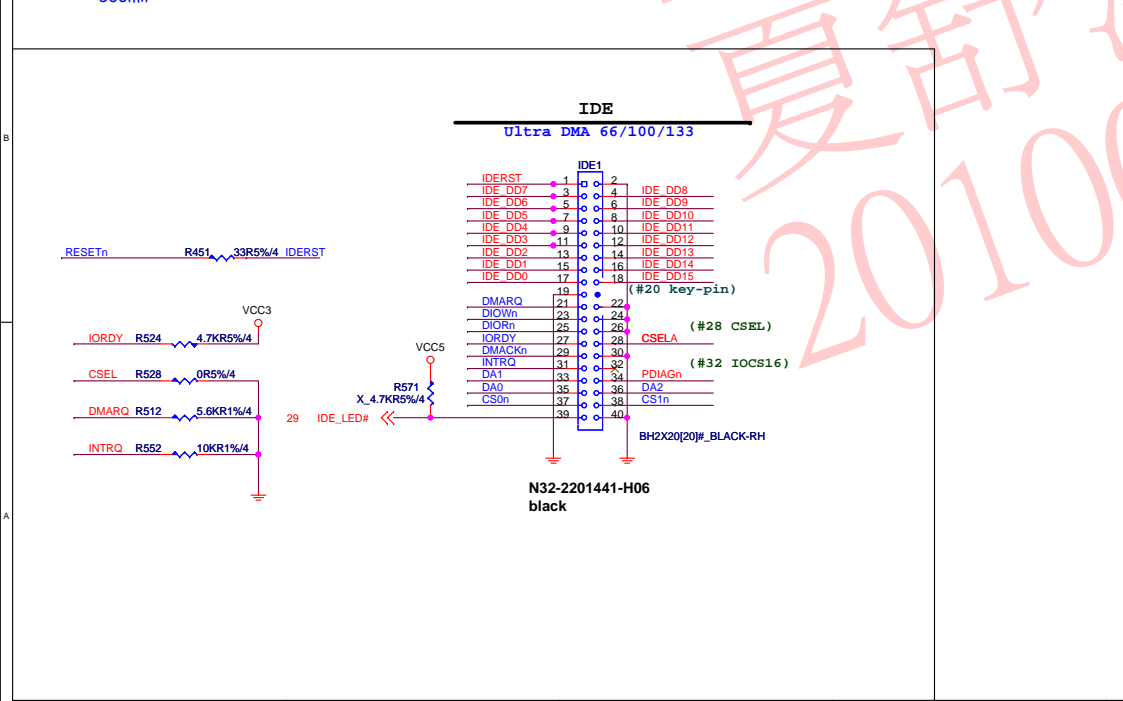
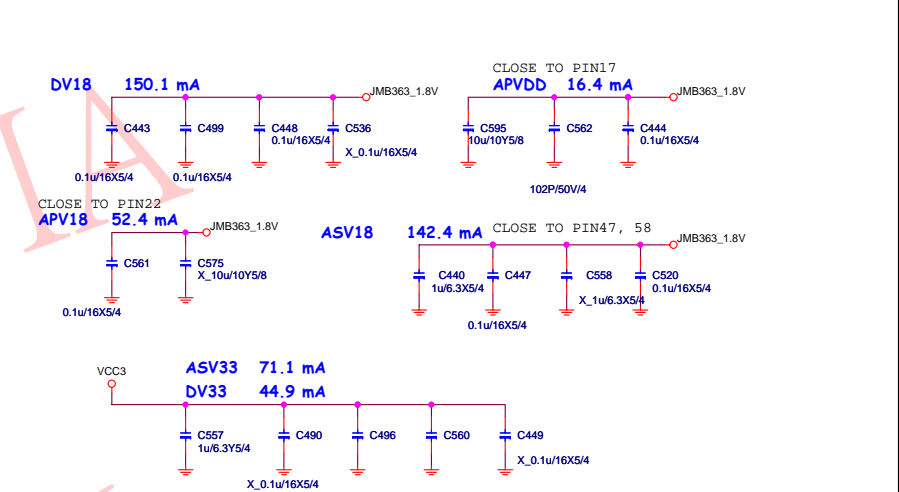
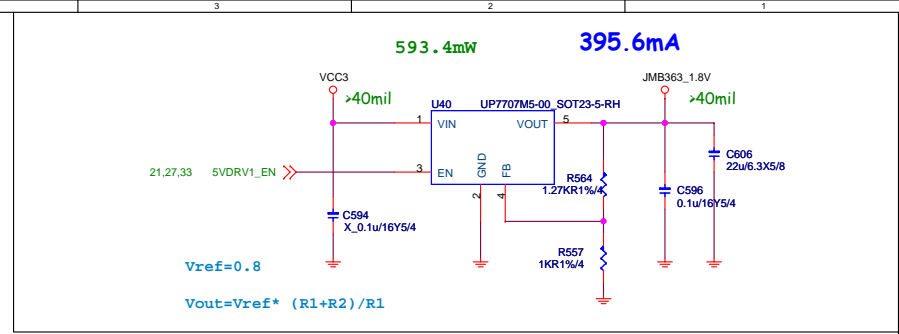
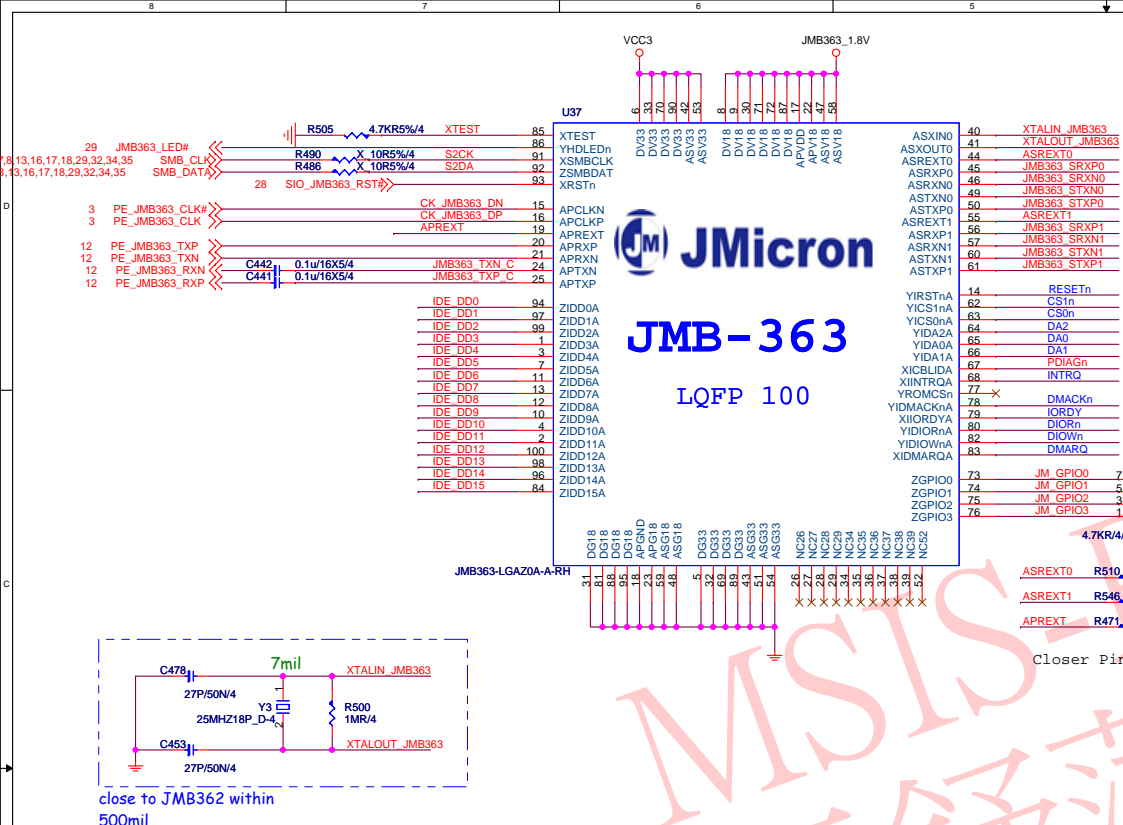
Giga-Lan		10/100-Lan	
N58-22F0081-S42		N58-22F0061-S42 N58-22F0061-F02	
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	100	Green
100	Green	10	None
10	None		
19		19	
20	Yellow	20	Yellow
21	Orange	21	
22	Green	22	Green



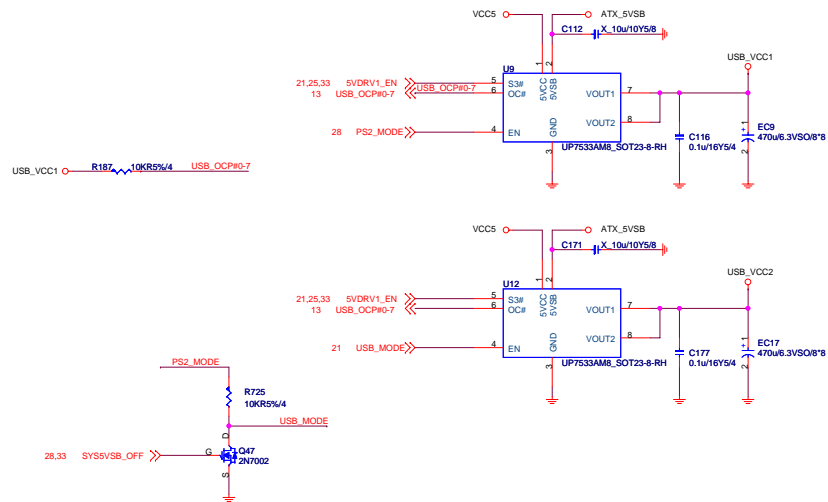
MICRO-STAR INT'L CO.,LTD

MS-7640

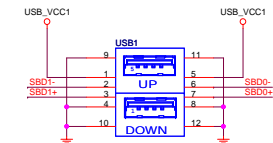
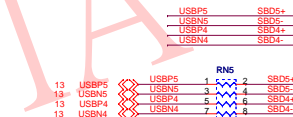
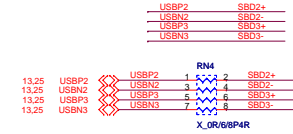
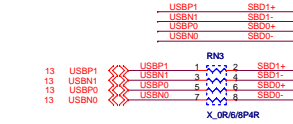
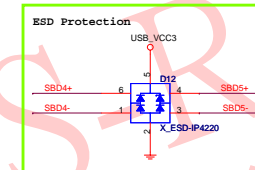
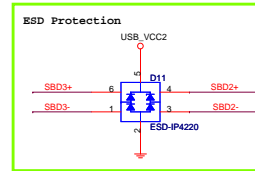
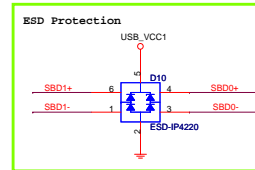
Size Custom	Document Description LAN2 RTL 8111E	Rev 1.4
Date: Tuesday, June 22, 2010		Sheet 24 of 42



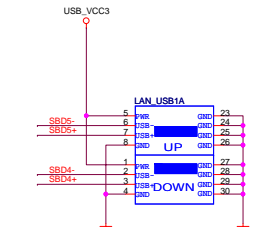
POWER CIRCUIT FOR USB PORT 0,1



REAR PANEL USB CONNECTOR FOR USB PORT 0 - 7

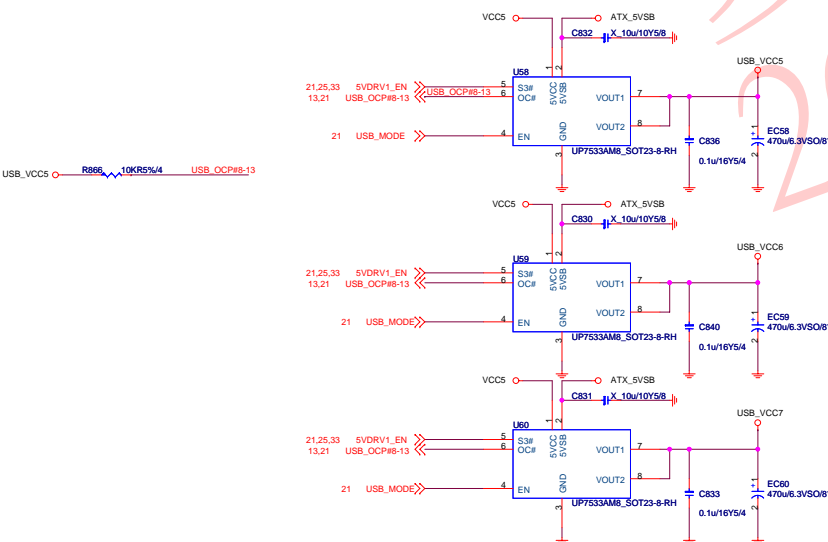


N58-12M0011-I60

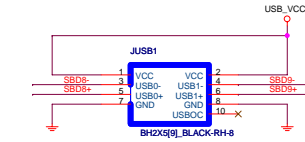
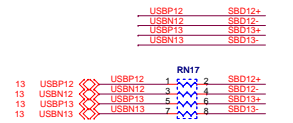
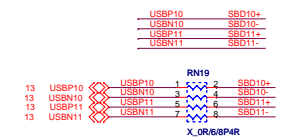
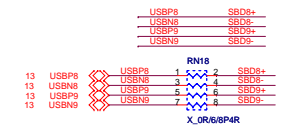
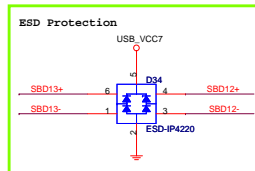
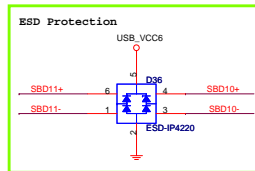
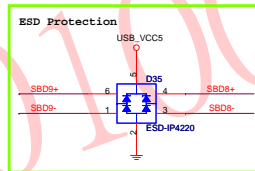


R45_USBX2_LED2_TX-GIGA-RH-1
N58-12M0011-I60

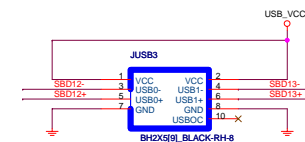
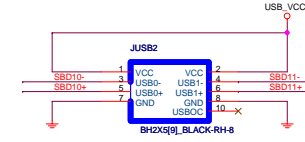
POWER CIRCUIT FOR USB PORT 8,9,10



FRONT PANEL USB CONNECTOR FOR USB PORT 8 - 11



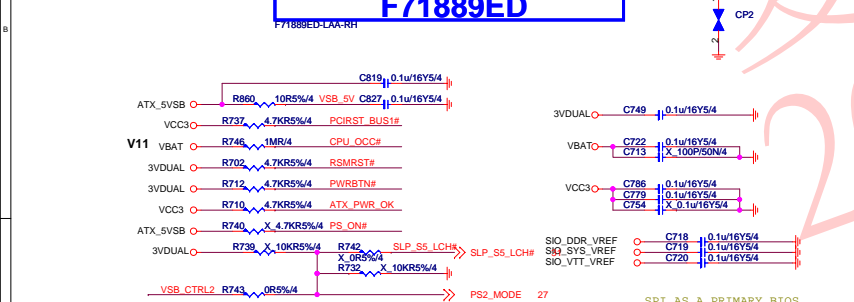
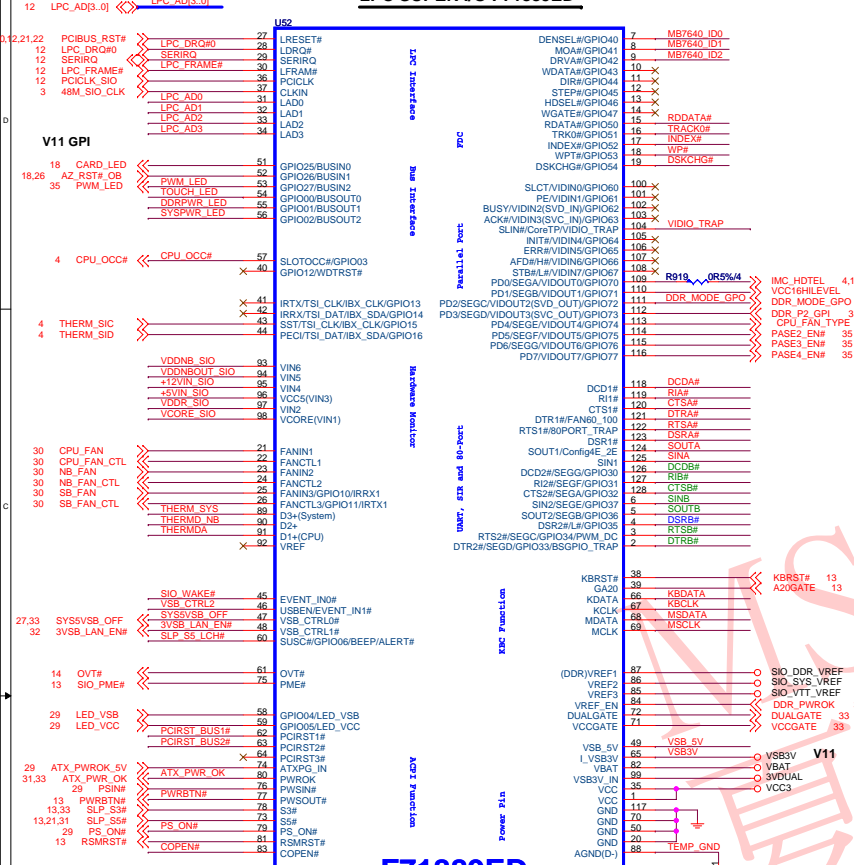
N31-2051581-H06
N32-2051371-H06(Blk, housing)



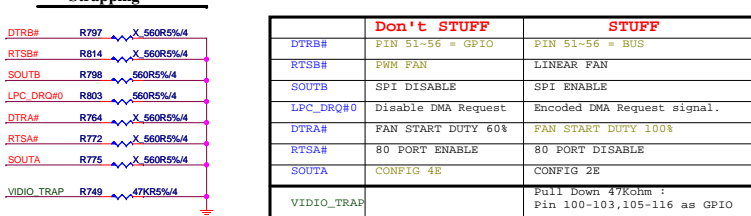
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Super I/O

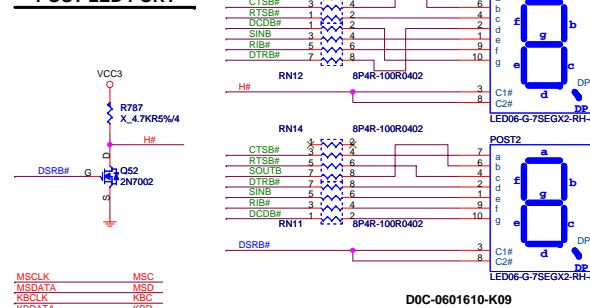
LPC SUPER I/O F71889ED



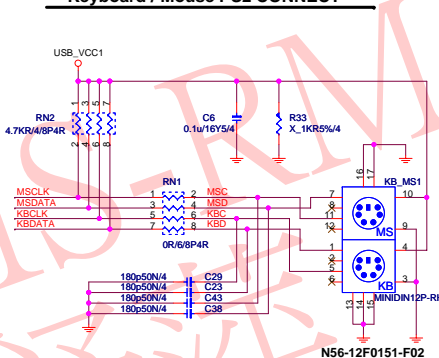
Strapping



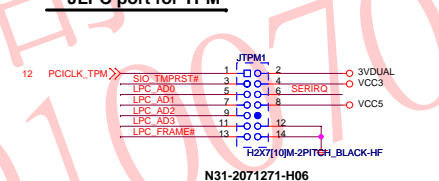
POST LED PORT



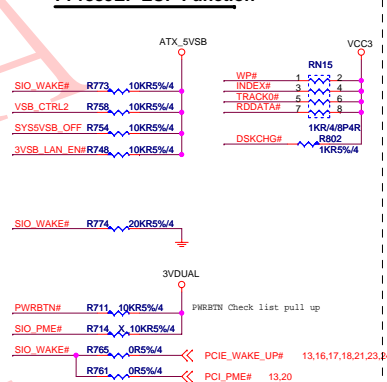
Keyboard / Mouse PS2 CONNECT



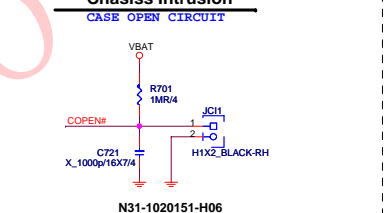
JLPC port for TPM



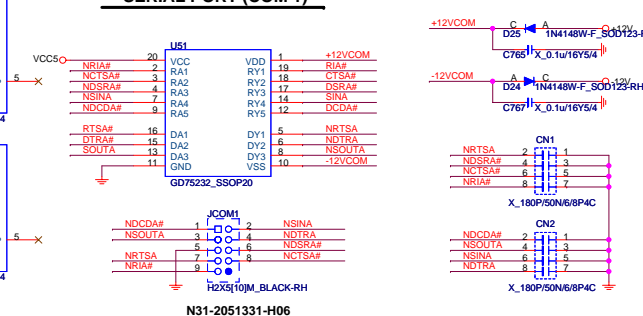
71889EF EUP Function



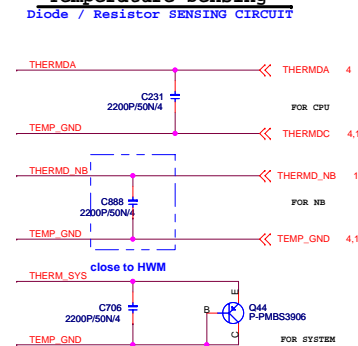
Chassis Intrusion



SERIAL PORT (COM 1)

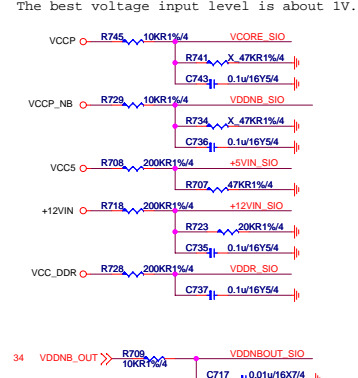


Temperature Sensing

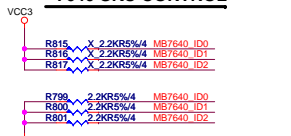


VOLTAGE SENSING(H/W Monitor)

The best voltage input level is about 1V.



7640 SKU CONTROL



2	1	0	ROM TYPE
0	0	0	V1.1 ALC889+BIOS FAN PATCE
0	0	1	V1.2 MCU+ALC889
0	1	0	V1.3 ALC892
0	1	1	V1.4 ALC889
1	0	0	V1.4 ALC892
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

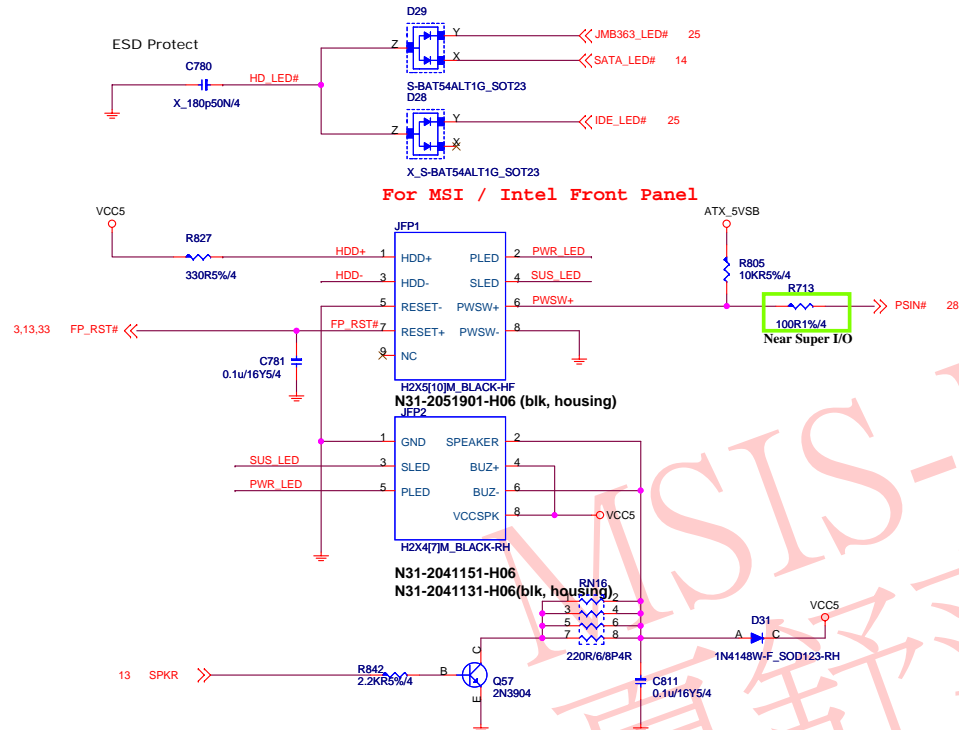


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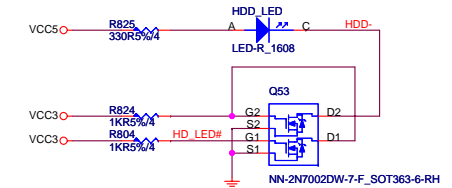
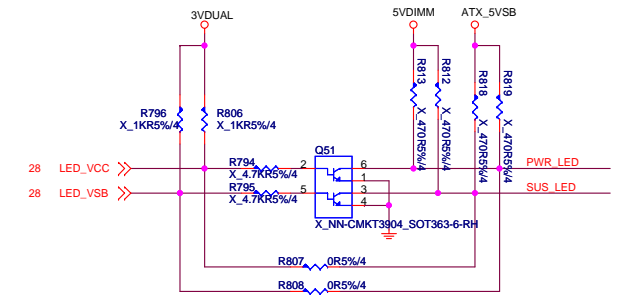
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Size	Document Description
Custom	SIO - F71888E/ EDD/ KRMS

ATX connector / Front Panel

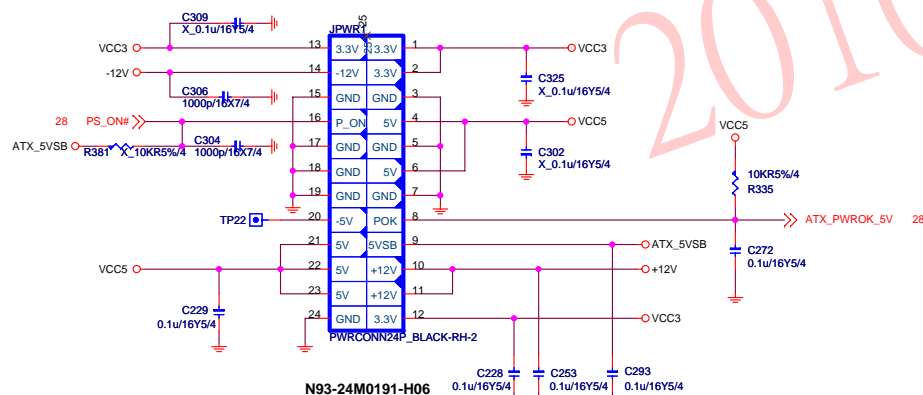
Intel Front Panel



LED (for Fintek 71889)

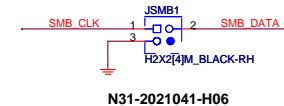


ATX Power Connector (2x20)



3,7,8,13,16,17,18,25,32,34,35
3,7,8,13,16,17,18,25,32,34,35

SMB_CLK
SMB_DATA

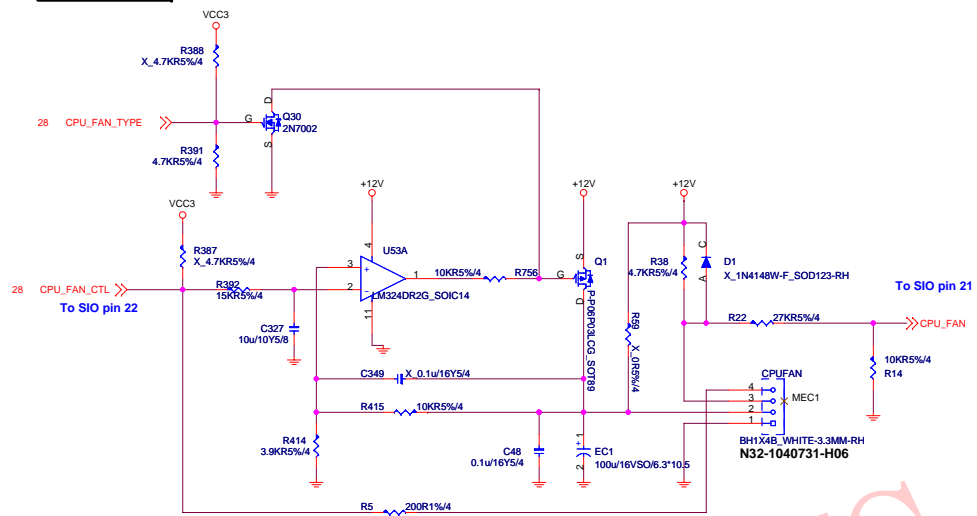
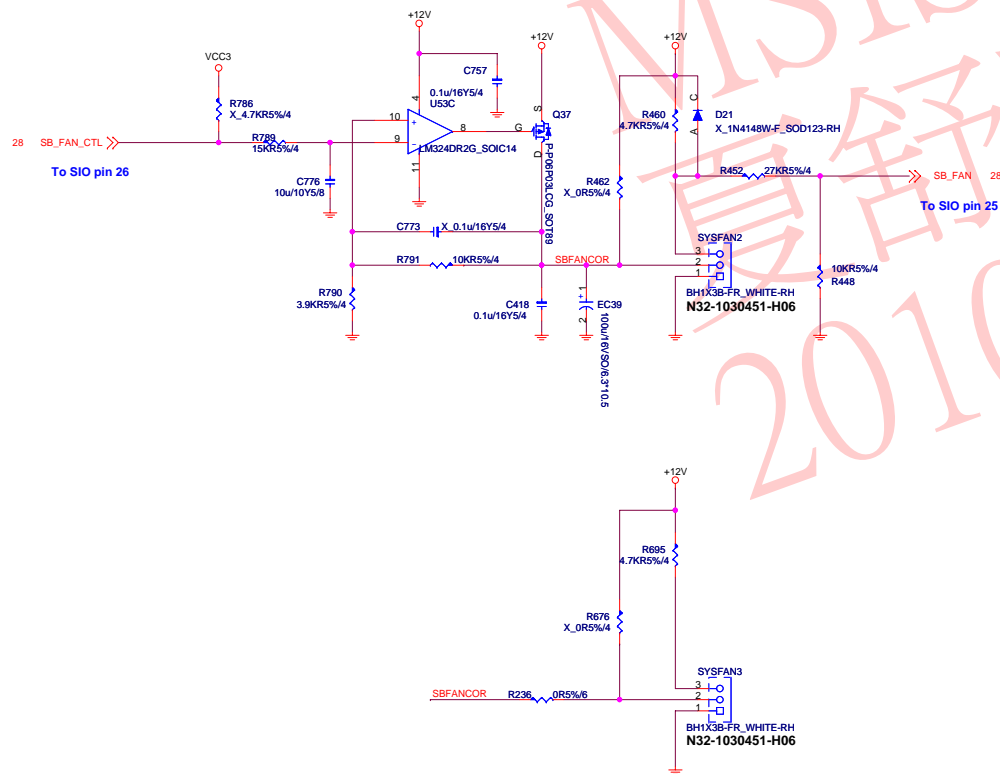


MICRO-STAR INT'L CO.,LTD

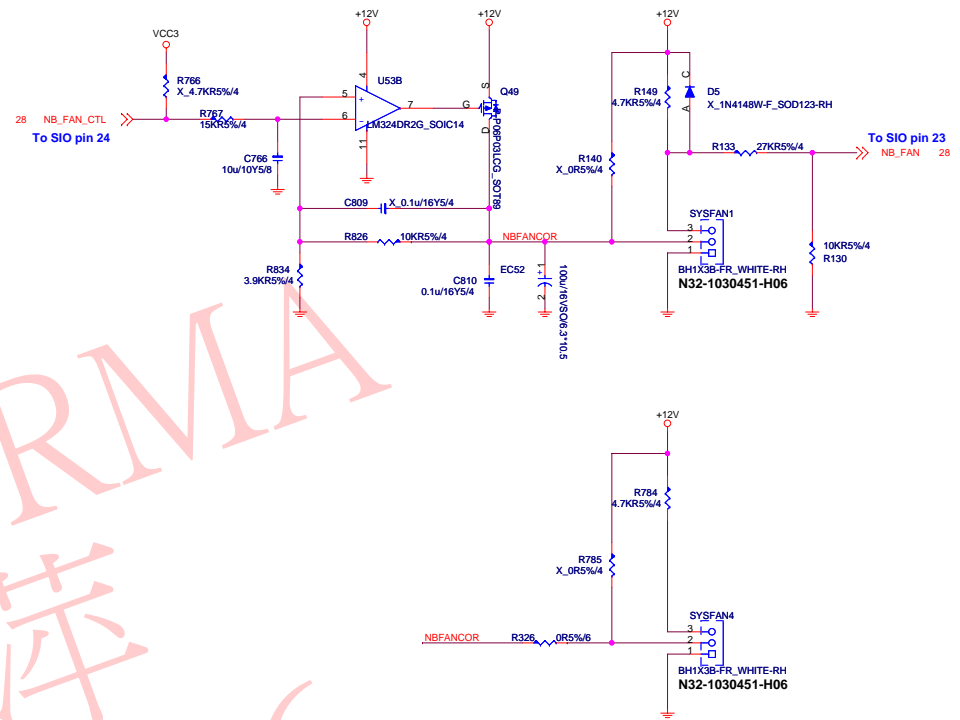
MS-7640

Size	Document Description	Rev
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CPU FAN

**SB FAN**

NB FAN

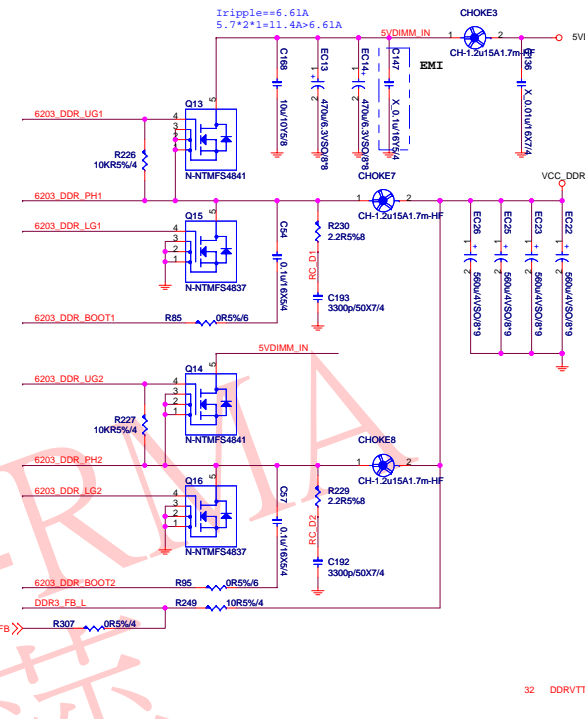
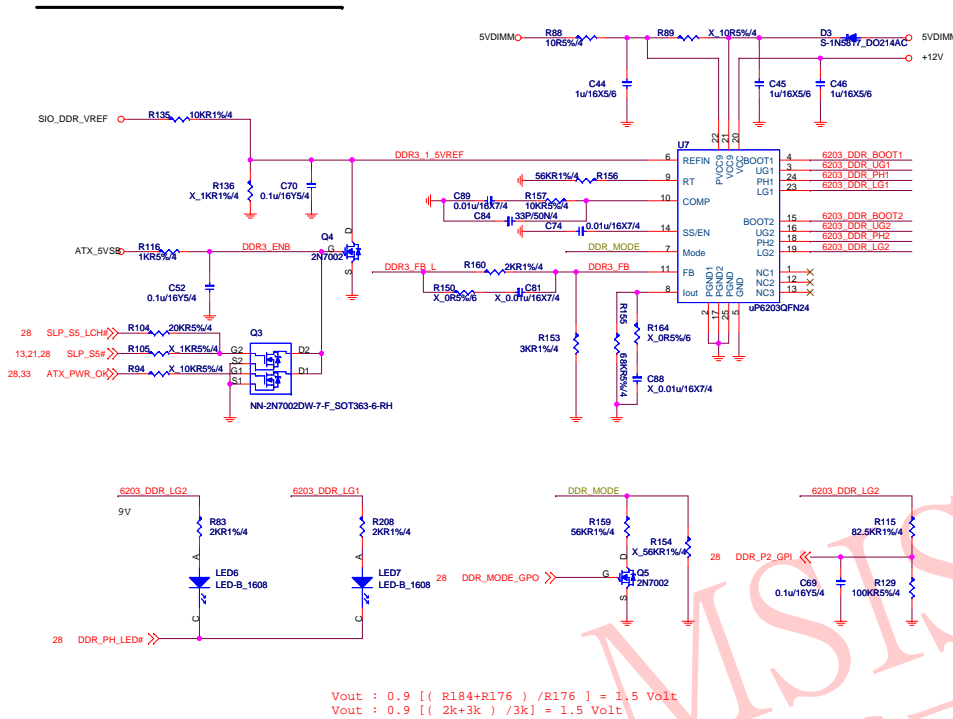


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DDR III 1.5V POWER



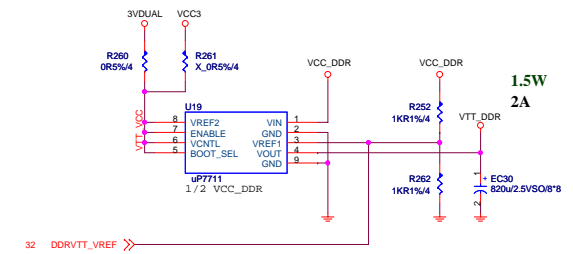
8.25A
80%, 41.25W

20+2=22A
33W

1.8A*6+0.2075A*6+6A=6A+
10.8A+1.245A=18.045A

DDR VTT Power

To CPU Copper trace width > 250mils , Fill
island behind DIMM > 400mils .

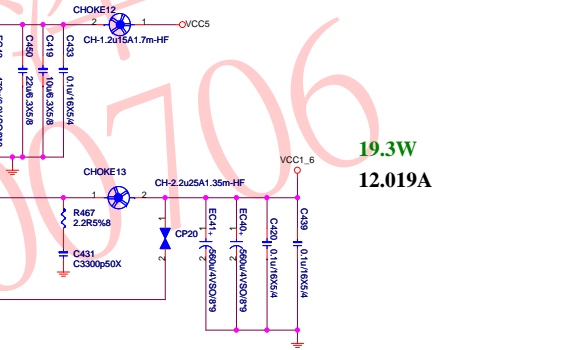
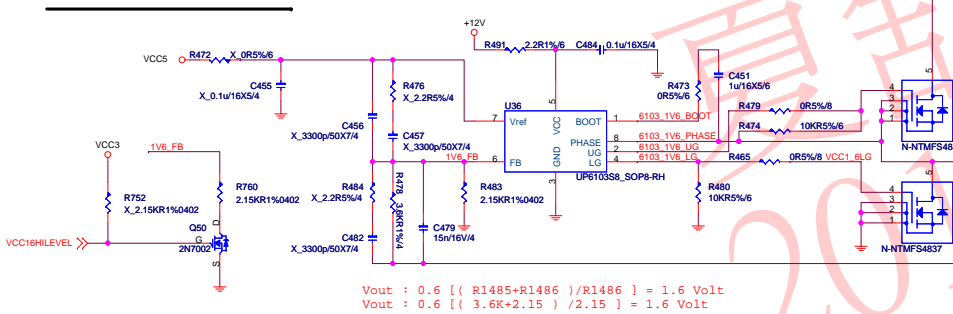


1.5W
2A

SYSTEM 1.6V POWER

80%, 31.85W

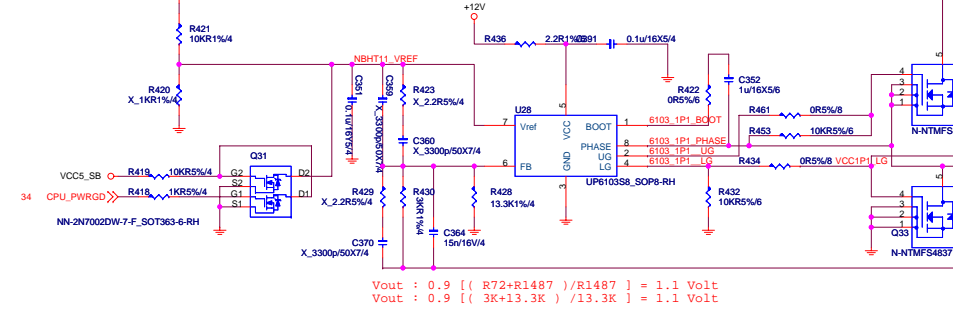
6.3A




19.3W
12.019A

VCC1_6 change to 2.12V

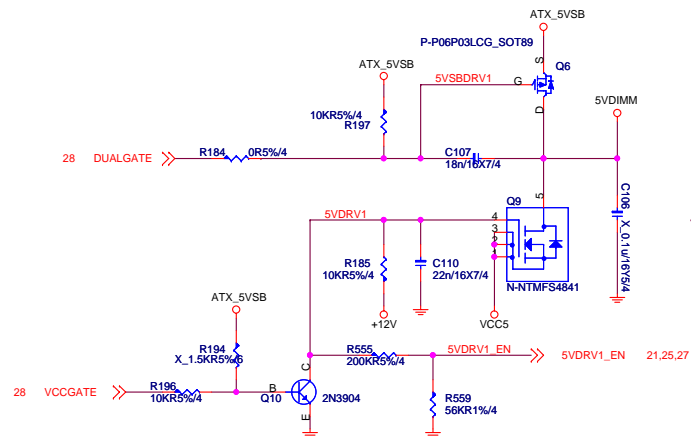
V1P1_NBCORE, 3.4A S0 / S1 For NB VDDC 1.1V
VDD1P1_NBHT, 1.8A S0 / S1 For NB VDDHTRX 1.1V



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	MS-7640		
	Size Custom	Document Description SYS. 2 POWER - LDO/ Regulator	Rev 1.4
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5VDIMM FOR DDR

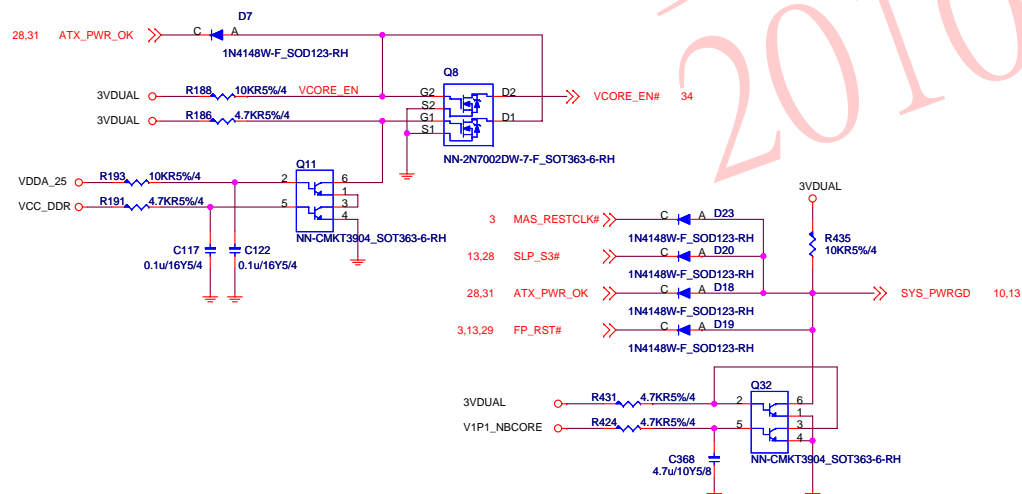
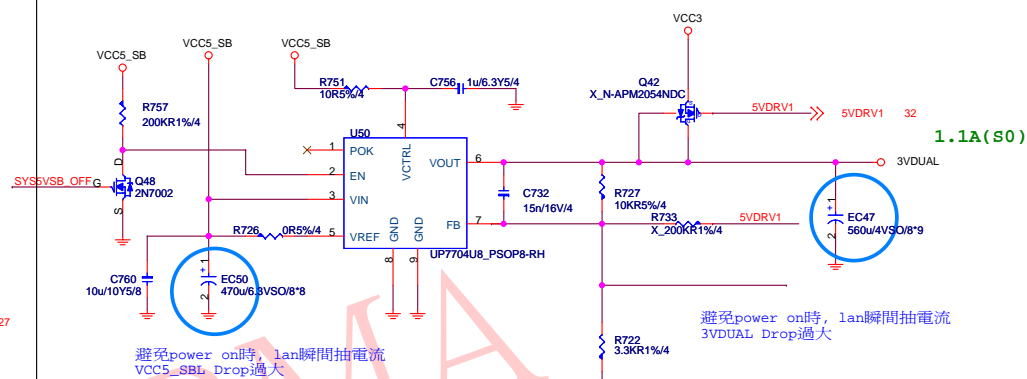
```
H:Support S0/S3/S5
L:Support S0/S3
```



3VDUAL,
1.017A

S0 - S5

For SB USB 1.2V, 310mA
For SB 3VDUAL 3.3V, 712mA



5VSB Power Switch

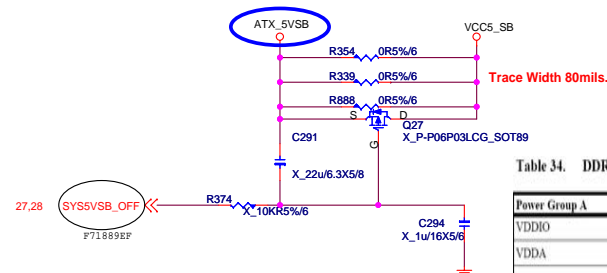

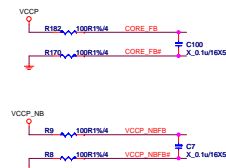
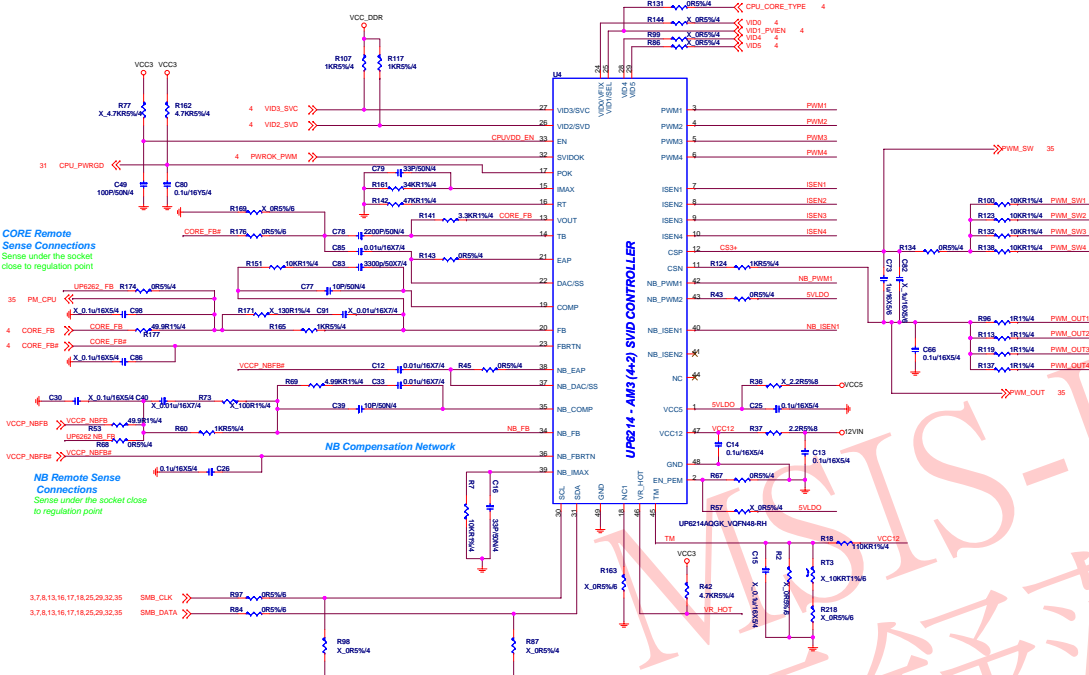


Table 34. DDR3 Power Sequencing Group Definitions

Power Group A		Power Group B	
VDDIO		VDD	
VDDA		VDDNB	
		VLDI	
		VDDR	

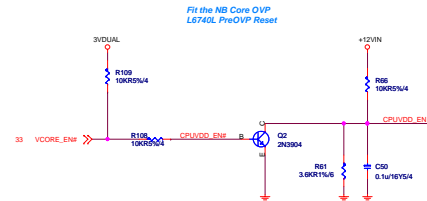
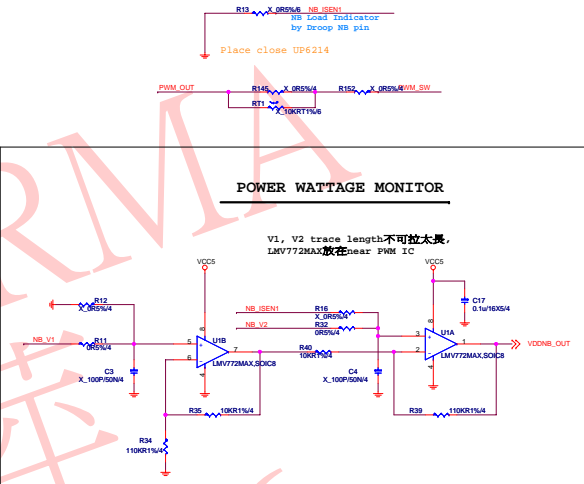
	MICRO-STAR INT'L CO.,LTD		
	MS-7640		
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UPI up6214+Dr-MOS(R2J20604NP)



Place close UP621.

place close UP6214

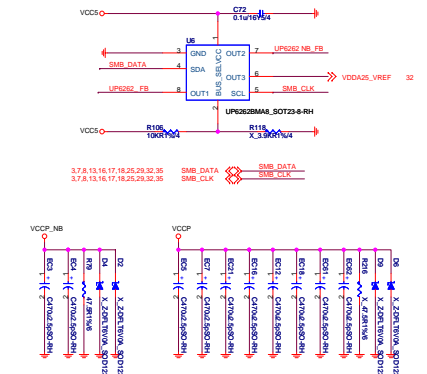


ADDRESS	0x6A	0X68	0x66	0x64	0x62	0x60
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

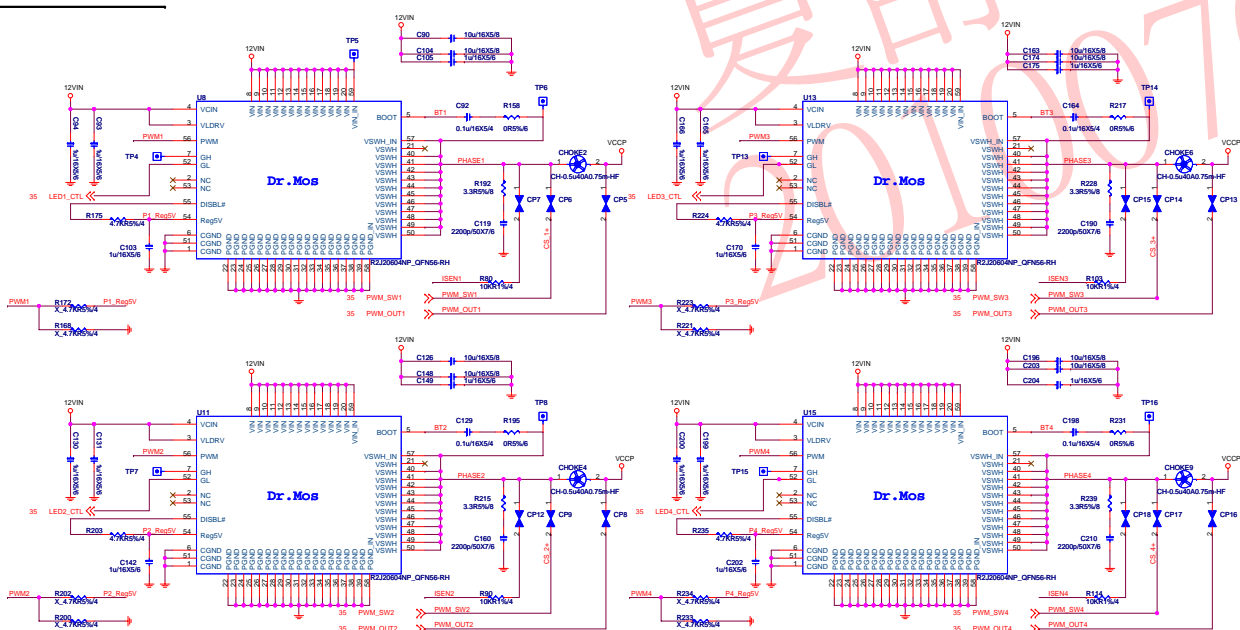
up6262不上件, R1355.R1444 不上件

100 Vcc5

0 x 60 : RH = 10K, RL = open



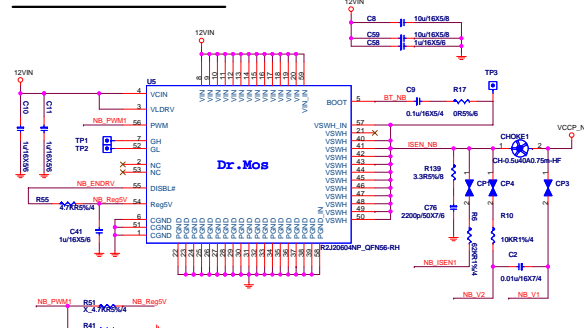
CPU_VDD_RUN



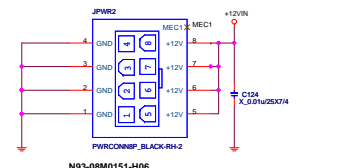
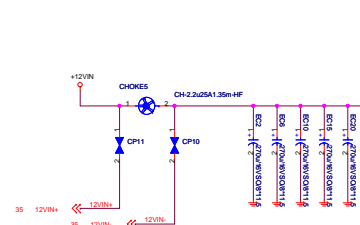
EM

PHASE1	C95	X 0.1u/16V5%
PHASE2	C133	X 0.1u/16V5%
PHASE3	C167	X 0.1u/16V5%
PHASE4	C201	X 0.1u/16V5%
ISEN_NB	C27	X 0.1u/16V5%

CPU_VDDNB_RUN



ATX Power Connector (2x4)



POWER METER

SMBUS ADDRESS 0X8C

CLOSE L17

電壓測點

Voltage TEST POINTS

VCCP	C97	X 4.7u6.3X5/8
VCCP_NB	C87	X 4.7u6.3X5/8
VCC_DDR	C221	10u6.3X5/8
V1P1_NBCORE	C395	X 4.7u6.3X5/8
V1P1_NBPCIE	C298	X 4.7u6.3X5/8
VDD1P2_NBHT	C211	X 4.7u6.3X5/8
1P1V_SB_CORE	C477	X 4.7u6.3X5/8

PWM LED CONTROL

Dr.MOS 關閉順序 2 4 3 1
PHASE LED 切換順序 2 4 3 1

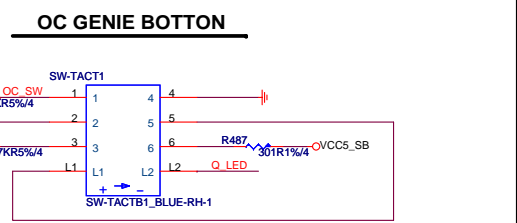
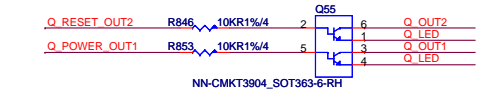
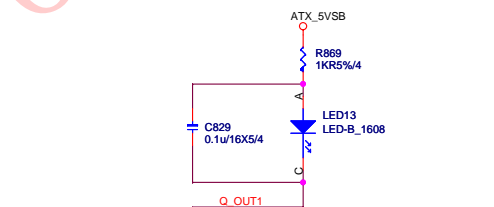
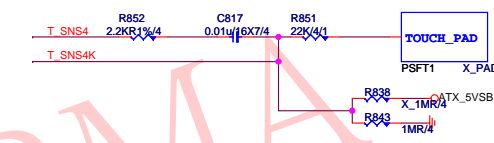
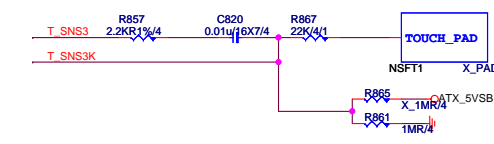
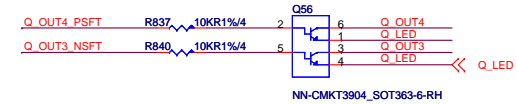
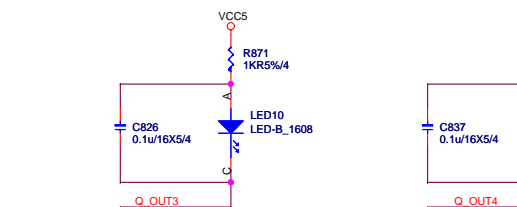
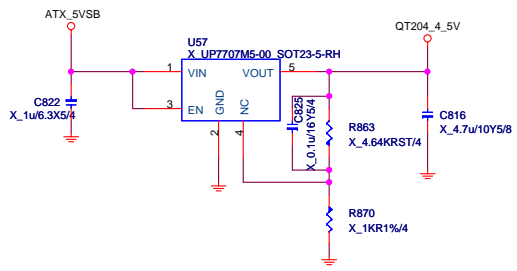
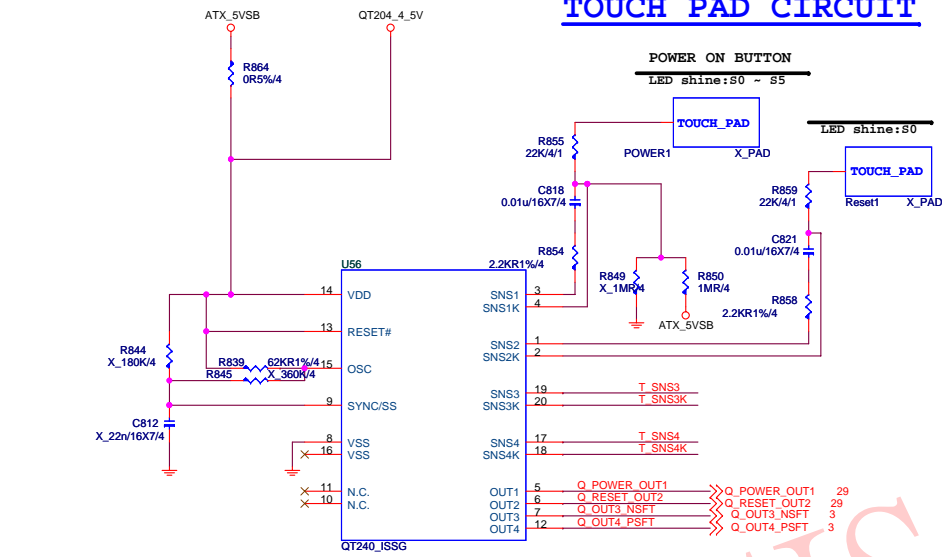


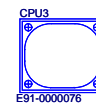
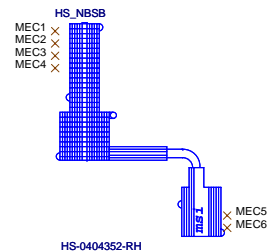
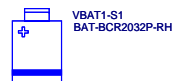
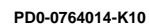
MICRO-STAR INT'L CO.,LTD

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TOUCH PAD CIRCUIT



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